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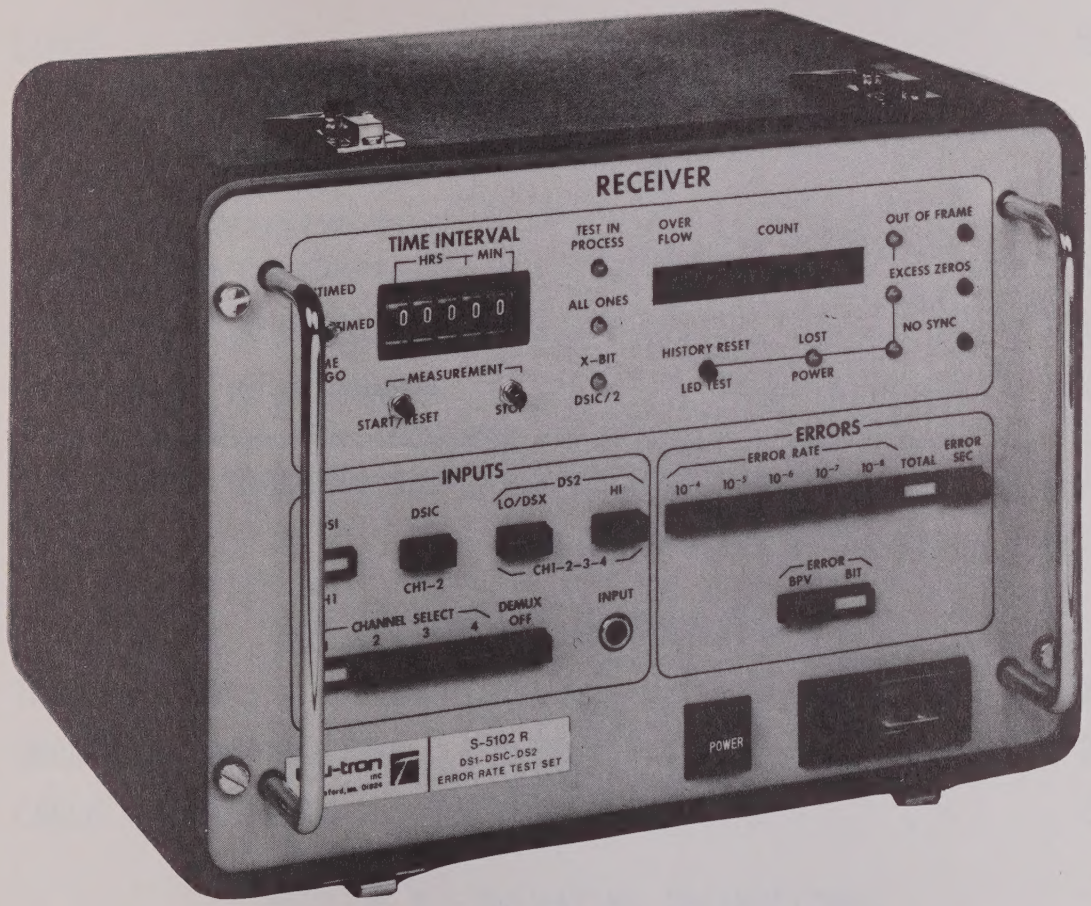
S5102

ERROR RATE TEST SET
RECEIVER
INSTRUCTION MANUAL
FORM 0196-0382C

dustrial Ave., Chelmsford, MA 01824

tau-tron



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S5102

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RECEIVER
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FORM 0196-0382C

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SECTION I

INTRODUCTION

GENERAL DESCRIPTION

THIS MANUAL PROVIDES THE INFORMATION REQUIRED TO INSTALL, OPERATE, AND MAINTAIN THE MODEL S5102 ERROR RATE TEST SET RECEIVER (HEREINAFTER REFERRED TO AS THE "RECEIVER TEST SET").

THE RECEIVER TEST SET MAY BE USED SEPARATELY OR IN CONJUNCTION WITH THE S5102 TRANSMITTER OR KS-20775L1/L2 ERROR RATE TEST SETS WHICH ARE DESIGNED TO TEST T-CARRIER COMMUNICATIONS EQUIPMENT AT STANDARD DS1, DS1C, OR DS2 RATES UTILIZING ERROR COUNTING TECHNIQUES.

THE RECEIVER TEST SET WILL RECEIVE STANDARD DS1 (1.544MB/S), DS1C (3.152MB/S), AND DS2 (6.312MB/S) PCM TRANSMISSION RATES THROUGH M1C, M12, AND THE LOW SPEED SECTIONS OF M13 MULTIPLEXERS.

THE RECEIVED DS1 SIGNAL IS A STANDARD $2^{20}-1$ DATA SEQUENCE WITH 15 ZERO SUPPRESSION. THE RECEIVER DEMULTIPLEXES THE DS1C AND DS2 SIGNALS TO THE INDIVIDUAL DS1 CHANNEL RATE TO EXAMINE THE DATA. THE RECEIVER DS1C INPUT CONTAINS TWO INDIVIDUAL CHANNELS OF THE DS1 DATA SEQUENCE WITH DS1C FRAMING BITS. IT CAN ALSO EXAMINE THE DS2 INPUT WHICH CONTAINS FOUR INDIVIDUAL CHANNELS OF THE DS1 DATA SEQUENCE WITH DS2 FRAMING BITS.

PHYSICAL DESCRIPTION

THE RECEIVER IS CONTAINED IN A 9¼" (H) X 13" (W) X 11 3/4 " (D) ENCLOSURE THAT WEIGHS APPROXIMATELY 16 LBS. (REFER

TO FIG 1-1). ALL MAJOR CONTROLS AND INDICATORS REQUIRED TO OPERATE THE TEST SET ARE LOCATED ON THE FRONT PANEL AND DESCRIBED IN SECTION 3. AUXILIARY CONNECTORS ARE PROVIDED ON THE REAR OF THE UNIT AND ARE USED AS SIGNAL SOURCES FOR TESTING PURPOSES IN CONJUNCTION WITH THE TRANSMITTER.

THE TEST SET REQUIRES ONLY THE APPLICATION OF 155 VAC, 60 Hz POWER THROUGH A 3/4A SLOW BLOW FUSE (1) ON THE FRONT PANEL. POWER IS APPLIED TO THE FRONT PANEL THROUGH THE USE OF THE POWER CABLE SUPPLIED WITH THE TEST SET.

THE DC POWER SUPPLY THAT SUPPLIES THE REQUIRED VOLTAGES TO THE PRINTED CIRCUIT BOARDS IS MOUNTED IN THE TEST SET AS SHOWN IN FIGURE 1-1. A DETAILED DESCRIPTION OF THE POWER SUPPLY IS PROVIDED IN APPENDIX A. DC POWER DISTRIBUTION TO THE PC BOARDS IS PROVIDED THROUGH THE PRINTED CIRCUIT BACK-PLANE THAT INTERCONNECTS THE PRINTED CIRCUIT BOARDS.

THE TEST SET MEETS OR EXCEEDS ALL BELL SYSTEM TEST SET DESIGN REQUIREMENTS, INCLUDING ROUNDED EDGES ON ALL OUTER SURFACES, PANEL DESIGNATIONS THAT CAN BE EASILY READ UNDER LOW LEVEL LIGHT CONDITIONS, PERMANENT OPERATIONAL INSTRUCTIONS APPLIED TO THE OUTER SURFACE OF THE ENCLOSURE, GUARD HANDLES TO PRO-TECT FRONT-PANEL CONTROLS AND INDICATORS, RUBBER FEET ON BOTTOM AND BACK OF THE TEST SET, AND DETACHABLE COVER AND POWER CORD.

SOLID-STATE AND DISCRETE COMPONENTS ARE EMPLOYED THROUGHOUT THE RECEIVER WITH EXTENSIVE USE OF INTEGRATED CIRCUITS FOR EXTENDED RELIABILITY. PRINTED CIRCUIT BOARDS ARE CONNECTED INTO THE SYSTEM BY A PRINTED CIRCUIT BACKPLANE MOUNTED ON THE BOTTOM OF THE TEST SET. INTERCONNECTION FROM THE CIRCUIT

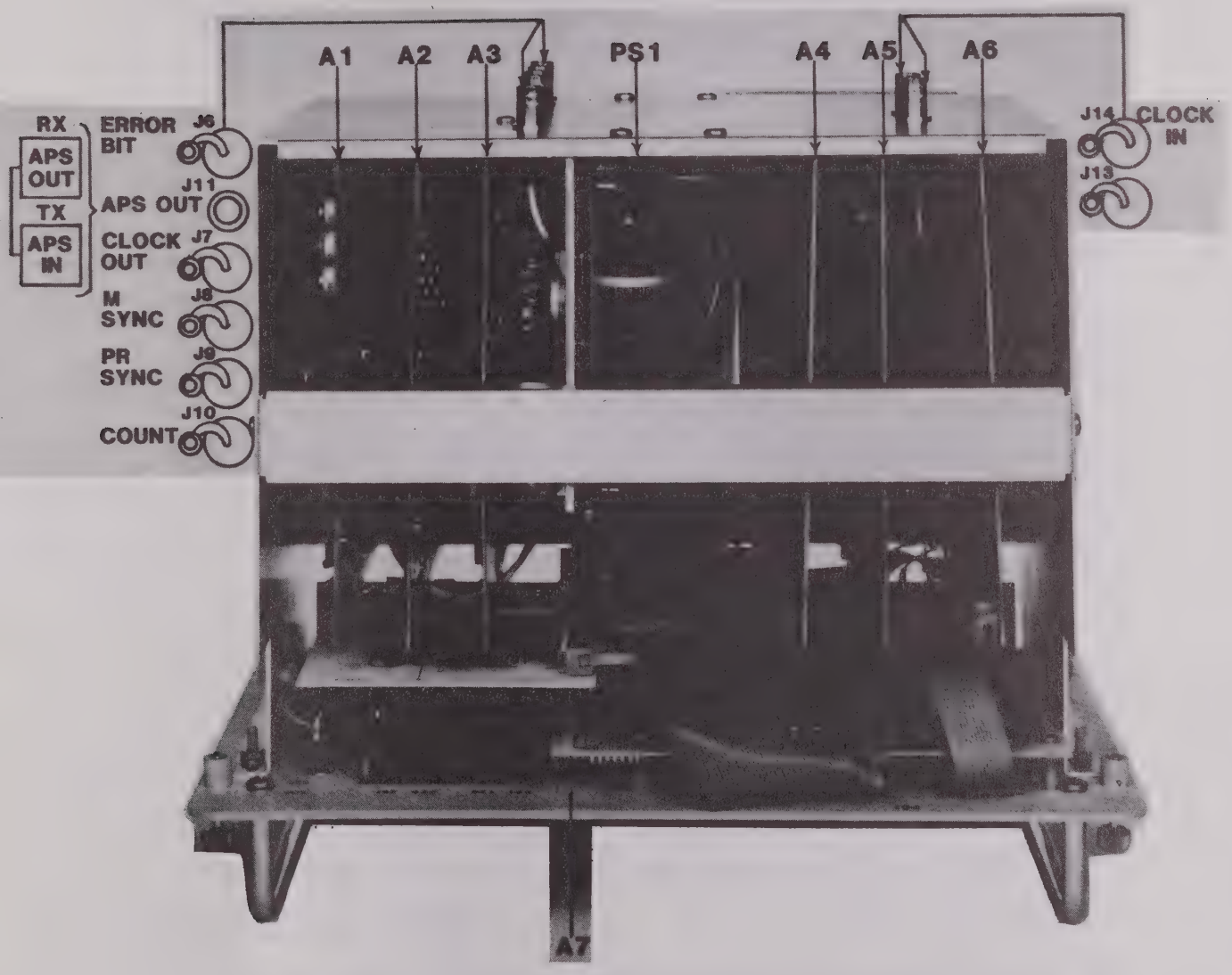


FIGURE 1-1 RECEIVER TEST SET MAJOR COMPONENTS
(TOP VIEW, ENCLOSURE REMOVED)

BOARDS TO THE FRONT PANEL UTILIZE RIBBON CABLES WITH DUAL IN-LINE CONNECTORS.

THE LOCATIONS OF THE MAJOR COMPONENTS IN THE TEST SET ARE LISTED IN FIG. 1-1 AND DEFINED IN TABLE 1-1.

FUNCTIONAL DESCRIPTION

THE TEST SET WILL ACCEPT A WIDE RANGE OF INPUT SIGNALS FROM BELL-COMPATIBLE COMMUNICATIONS TERMINAL AND LINE EQUIPMENT THAT CONFORMS TO DS1 (1.544 MB/S), DS1C (3.152 MB/S), AND DS2 (6.312 MB/S) DATA RATES.

THE RECEIVER WILL EVALUATE THE DATA FORMATS AT EACH OF THE DATA RATES AND DISPLAY ANY RESULTANT BIT ERRORS, BIPOLAR LINE CODE VIOLATIONS, EXCESSIVE STRINGS OF ZERO'S, AND DATA WITH AN ALL ONE'S LOGIC CONTENT.

THIS IS ACCOMPLISHED BY DECODING THE BIPOLAR INPUT SIGNAL, EXTRACTING CLOCK AND FRAME BITS, DEMULTIPLEXING AND DESTUFFING THE DS1 SEQUENCES CONTAINED IN THE INPUT SIGNAL. THE INPUT SIGNAL IS MONITORED FOR BIPOLAR VIOLATIONS AND THE DEMULTIPLEXED DATA ARE CHECKED FOR BIT ERRORS. THE CHOICE OF WHICH TYPE OF ERROR TO BE COUNTED OR DISPLAYED IS SELECTED ON THE FRONT PANEL.

THE ERROR COUNTER MAY BE SELECTED TO RECORD TOTAL ERRORS (UP TO 99,999), ERRORS AT RATES OF FROM 10^{-4} THROUGH 10^{-8} (IN 10^{1} INCREMENTS), OR TOTAL ERROR SECONDS (UP TO 99,999). TOTAL ERRORS AND ERROR-SECONDS MAY BE TIMED IN INCREMENTS OF HOURS AND MINUTES UP TO 999 HOURS, 99 MINUTES, OR ALLOWED TO FREE-RUN INDEFINITELY UNTIL MANUALLY RESET.

TABLE 1-1
MAJOR COMPONENTS

INDEX NUMBER	COMPONENTS
A1	INPUT AMPLIFIER/CLOCK RECOVERY PRINTED CIRCUIT BOARD (PC6).
A2	FRAME SYNC PRINTED CIRCUIT BOARD (PC5).
A3	DEMULTIPLEXER PRINTED CIRCUIT BOARD (PC7).
A4	PR SYNC PRINTED CIRCUIT BOARD (PC4).
A5	ERROR ACCUMULATOR PRINTED CIRCUIT BOARD (PC3).
A6	TIMER PRINTED CIRCUIT BOARD (PC8).
A7	DISPLAY PRINTED CIRCUIT BOARD (PC1).
PS1	DC POWER SUPPLY (REFER TO APPENDIX A).
J6	BIT ERROR OUTPUT CONNECTOR.
J7	CLOCK OUTPUT CONNECTOR, DEPENDENT UPON SELECTED RATE.
J8	"M" SYNC OUTPUT CONNECTOR, FOR TEST PURPOSES.
J9	"PR" CONNECTOR, FOR TEST PURPOSES.
J10	COUNT CONNECTOR, FOR TEST PURPOSES.
J11	APS OUT WECO 310-TYPE CONNECTOR,FOR TEST OF AUTOMATIC PROTECTION SWITCH.
J13	DATA IN CONNECTOR, FOR TEST PURPOSES.
J14	CLOCK IN CONNECTOR, FOR TEST PURPOSES.

OPERATING REQUIREMENTS

THE FOLLOWING PARAGRAPHS BRIEFLY COVER THE OPERATING REQUIREMENTS FOR THE RECEIVER TEST SET. ALL GENERAL REQUIREMENTS THAT ARE NORMALLY ASSOCIATED WITH ELECTRONIC EQUIPMENT WILL APPLY TO THIS UNIT.

Personnel Requirements

The Test Set may be efficiently operated and adequately maintained by personnel skilled in electronic technology and digital logic circuitry. They should also be familiar with the required communications equipment with which the Test Set is designed to interface.

Environmental Requirements

For most efficient operation, the following conditons are recommended:

- Ambient temperature between 0^{o} C. and 50^{o} C.
- Relative Humidity of 10% to 95% (non-condensing).

Equipment Required But Not Supplied

Normal operation of the Test Set requires cables for interconnecting the Test Set to the communications equipment with which it will be operated. Section 2 of this manual provides a description of the required cables and their part numbers. Table 5-1 in Section 5 lists the test equipment required for maintenance.

WARRANTY

All Tau-Tron products are warranted against any defects in material and workmanship. This warranty applies for one year from the date of delivery for all Tau-Tron manufactured products. The warranty period for OEM products sold by Tau-Tron

WILL DEPEND ON THE ORIGINAL OEM WARRANTY (CONSULT THE FACTORY FOR SPECIFIC PRODUCTS). WE WILL REPAIR OR REPLACE PRODUCTS WHICH, UPON OUR EXAMINATION, PROVE TO BE DEFECTIVE DURING THE WARRANTY PERIOD.

NO OTHER WARRANTY, EXPRESS OR IMPLIED, INCLUDING FITNESS FOR PURPOSE, MERCHANTABILITY, OR OTHERWISE, IS GIVEN.

FOR ANY ASSISTANCE, CONTACT THE FACTORY AND BE PREPARED TO PROVIDE INSTRUMENT MODEL AND SERIAL NUMBERS AND ALL DETAILS REGARDING THE MALFUNCTION.

SECTION 2
INSTALLATION

INTRODUCTION

This section provides the information necessary to unpack and test the S5102 Receiver Test Set for normal operation.

UNPACKING INSTRUCTIONS

The Test Set is shipped in a corrugated container that has been lined with bubblewrap and sealed with pressure sensitive tape. Carefully cut the tape sealing the container and remove the protective material with the Test Set as a whole. Strip off the bubblewrap.

CABLE REQUIREMENTS

The 115 VAC input power cable that is connected to the front panel of the Test Set is the only cable supplied with the Test Set. The other cable requirements to operate the Test Set are those terminated in the WECO 310-compatible plugs and the BNC-type monitor plugs that connect to the rear of the Test Set. (Refer to Table 2-1.)

TABLE 2-1

CONNECTION AND CABLE REQUIREMENTS

Reference Designation	Qty	Location	Connector Plug and Functions
INPUT	1	Front Panel	WECO 310 (or equivalent connected to a 110 ohm balanced, twisted pair shielded cable for input. (Refer to Table 3-1 for functional definition of test set connector.)
APS OUT (J11)	1	Front Panel	
BIT ERROR (J6)	1	Rear Panel	RG 59 connector (or equivalent) Connected to a 75 ohm coaxial Cable to monitor internal test Set signals. (Refer to Table 3-1 for functional definition of test set connector.)
CLOCK (J7)	1	Rear Panel	
'M' SYNC (J8)	1	Rear Panel	
'PR' SYNC (J9)	1	Rear Panel	
COUNT (J10)	1	Rear Panel	
CLOCK IN (J14)	1	Rear Panel	
DATA IN (J13)	1	Rear Panel	

NOTE: The twisted pair shielded cable connected to the WECO connector MUST be balanced at 100 ohms to produce optimum output. (ADC products, PJ-8 series, or equivalent).

SECTION 3
OPERATING INSTRUCTIONS

INTRODUCTION

THE OPERATING INSTRUCTIONS FOR THE TEST SET ARE DESCRIBED IN THE FOLLOWING PARAGRAPHS BY FIRST DEFINING THE FUNCTIONS OF ALL THE CONTROLS AND INDICATORS THAT ARE ON THE FRONT PANEL. TABLE 3-1 AND FIGURE 3-1 CROSS-REFERENCE EACH FUNCTION TO ITS SPECIFIC PHYSICAL LOCATION.

ONCE THE OPERATOR IS FAMILIAR WITH THE LOCATION AND FUNCTION OF THE CONTROLS AND INDICATORS, THE OPERATIONAL PROCEDURES ARE DESCRIBED. THIS INCLUDES INITIAL TURN-ON PROCEDURES, TEST SET OPERATING PROCEDURES FOR DS1, DS1C, AND DS2 RATES, A SELF TEST, AND NORMAL SHUTDOWN OF THE EQUIPMENT.

CONTROLS AND INDICATORS

THE CONTROLS AND INDICATORS FOR THE TEST SET ARE LISTED IN TABLE 3-1 ACCORDING TO THE ETCHED NOMENCLATURE ON THE FRONT PANEL (E.G., TEST IN PROCESS, ALL ONES, ETC). THESE DEFINITIONS ARE FURTHER GROUPED INTO SUBDIVISIONS ON THE PANEL, I.E., TIME INTERVAL, INPUTS, AND ERRORS. TABLE 3-1 IS ALSO CROSS-REFERENCED ACCORDING TO INDEX NUMBER COLUMN WITH THAT OF FIGURE 3-1 IN AN EFFORT TO FAMILIARIZE THE OPERATOR WITH THE CONTROLS AND INDICATORS IN THE SHORTEST POSSIBLE TIME. THROUGHOUT THIS MANUAL, REFERENCE TO SPECIFIC CONTROLS AND INDICATORS WILL BE WRITTEN AS THEY APPEAR ON THE FRONT PANEL OF THE TEST SET.

TABLE 3-1

TEST SET RECEIVER OPERATING CONTROLS AND INDICATORS

INDEX NUMBER	CONTROL OR INDICATOR	FUNCTION
1	ALL ONES INDICATOR	ILLUMINATED WHEN SELECTED DS1 CHANNEL CONTAINS EXCESSIVE ONE'S DATA.
2	X-BIT (DS1C/2)	ILLUMINATED WHEN X-BIT IN THE FRAMING EQUALS A LOGIC ZERO FOR DS1C AND DS2.
3	COUNT INDICATOR	5-DIGIT COUNTER WITH OVERFLOW INDICATION FOR TOTAL AND ERROR SEC. 3-DIGIT WITH OVERFLOW FOR ERROR RATE.
4	HISTORY RESET/LED TEST PUSHBUTTON	ILLUMINATES ALL LED'S FOR LAMP TEST. RESETS THE HISTORY INDICATORS.
5	LOST POWER INDICATOR	INDICATES THAT POWER WAS LOST FOR AN INTERVAL OF TIME. IT IS RESET BY THE HISTORY RESET/LED TEST PUSHBUTTON OR START/RESET PUSHBUTTON
6	OUT OF FRAME INDICATOR	RED INDICATES CURRENT STATUS, AMBER INDICATES AT LEAST ONE OCCURRENCE OF LOST FRAME ERROR SINCE LAST MANUAL RESET. NOT APPLICABLE IN DS1.
7	EXCESS ZEROS INDICATOR	RED INDICATES CURRENT STATUS, AMBER INDICATES AT LEAST ONE OCCURRENCE OF EXCESS ZERO'S SINCE LAST MANUAL RESET. DS1-16 CONSECUTIVE ZERO'S DS1C-34 CONSECUTIVE ZERO'S DS2-6 CONSECUTIVE ZERO'S
8	NO SYNC	RED INDICATES CURRENT STATUS, AMBER INDICATES AT LEAST ONE OCCURRENCE OF LOST PSEUDORANDOM DATA SYNC.
9	ERROR RATE PUSHBUTTON (5)	SELECTS A BIPOLAR OR BIT ERROR RATE TIME PERIOD FROM 10^{-4} TO 10^{-8}.
10	TOTAL PUSHBUTTON	COUNTS INDIVIDUAL ERRORS UP TO 99,999 WITH OVERFLOW INDICATION.
11	ERROR SEC PUSHBUTTON	COUNTS SYNCHRONOUS ERRORED SECONDS UP TO 99,999 WITH OVERFLOW INDICATION.
12	ERROR BIPOLAR/BIT PUSHBUTTONS	SELECTS BIPOLAR OR BIT ERROR DETECTION.
13	POWER PUSHBUTTON/INDICATOR	APPLIES POWER TO THE TEST SET.
14	INPUT JACK	ACCEPTS INPUT VIA WECO 310-COMPATIBLE PLUG.
15	DEMUX OFF	INHIBITS FRAMING AND DEMULTIPLEXING FUNCTIONS.
	ON	ALLOWS ALL NORMAL FUNCTIONS ASSOCIATED WITH DEMULTIPLEXING DS1C AND DS2 SIGNALS.
16	CHANNEL SELECT	SELECTS CHANNELS 1 THROUGH 4. DS1 INPUT: CHANNELS 1 DS1C INPUT: CHANNELS 1, 2 DS2 INPUT: CHANNELS 1-4

TABLE 3-1

TEST SET RECEIVER OPERATING CONTROLS AND INDICATORS

INDEX NUMBER	CONTROL OR INDICATOR	FUNCTION
17	DS1/CH-1 CONTROLS	SELECTS RECEPTION AT DS1C RATE IN CHANNEL 1.
18	DS1C/CH-1-2 CONTROL	SELECTS RECEPTION AT DS1C RATE IN EITHER CHANNEL 1 OR 2.
19	LO/DSX (DS2) CONTROL	SELECTS RECEPTION AT DS2 RATE AND AT CABLE LENGTHS BETWEEN 1000' AND 2000'.
20	HI (DS2) CONTROL	SELECTS RECEPTION AT DS2 RATE AND HIGH AMPLITUDE.
21	TIME INTERVAL TOGGLE SWITCH	3-POSITION SWITCH: UNTIMED: MANAUL TIME MODE; TEST SET UNDER CONTROL OF OPERATOR. TIMED: TEST SET UNDER CONTROL OF PRE-SET TIME IN TIME INTERVAL SWITCH. TIME TO GO: CAUSES TIME REMAINING IN A TIMED TEST TO BE DISPLAYED.
22	TIME INTERVAL THUMB-WHEEL SWITCH	SELECTS THE HOURS AND MINUTES FOR A TIMED TEST THAT IS ACTIVATED BY START/RESET PUSHBUTTON, RANGE IS 999 HOURS, 99 MINUTES.
23	MEASUREMENT START/ RESET PUSHBUTTON	STARTS AND RESETS THE SAMPLE TIME SELECTED BY THE TIME INTERVAL THUMBWHEEL SWITCHES WHEN IN A TIME MODE. RESETS THE ERROR COUNTER TO ZERO. CLEARS HISTORY LAMPS. INITIATES A TOTAL ERROR SEC COUNT.
24	MEASUREMENT STOP PUSHBUTTON	TOTAL AND ERROR SECOND MEASUREMENTS CAN BE STOPPED BY DEPRESSING THIS BUTTON.
25	TEST IN PROCESS	ILLUMINATES FOR DURATION OF TIMED/UNTIMED TEST. FLASHES OFF MOMENTARILY FOR RATE MEASUREMENTS WHEN DISPLAY IS UPDATED.

TURN-ON PROCEDURE

THE ONLY EXTERNAL POWER REQUIREMENT FOR THE TEST SET IS THE POWER CABLE THAT IS PLUGGED INTO THE RECEPTACLE ON THE FRONT PANEL OF THE TEST SET. POWER IS APPLIED TO THE RECEIVER BY PUSHING THE POWER PUSHBUTTON/INDICATOR ON THE FRONT PANEL.

OPERATION

THE FIRST REQUIREMENT FOR RECEIVER OPERATION IS THE SELECTION

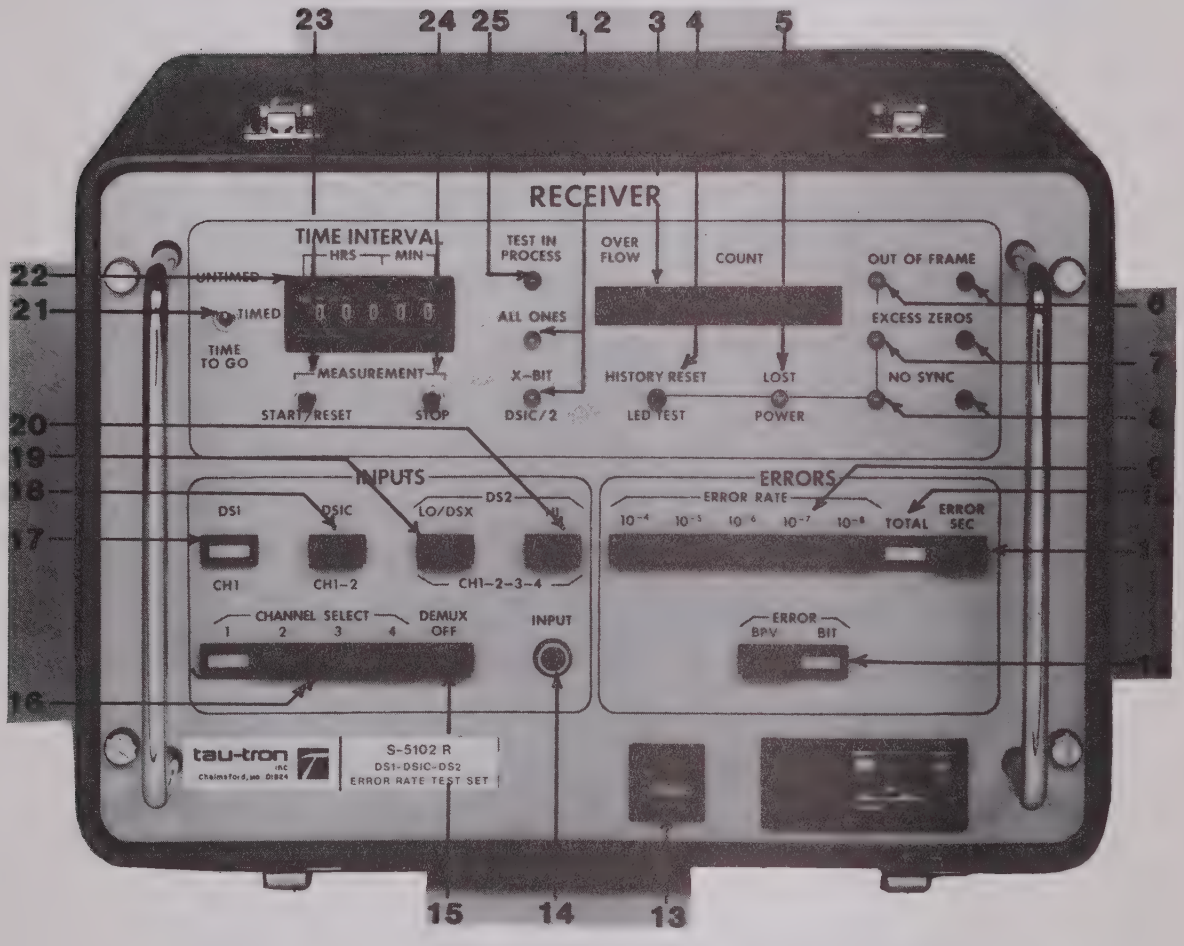


FIGURE 3-1 RECEIVER TEST SET OPERATING CONTROLS AND INDICATORS

OF THE APPROPRIATE DS RATE (DS1, DS1C, OR DS2) INPUT LEVEL (HI, DSX, OR LO) AND CHANNEL (1 THROUGH 4) ON THE FRONT PANEL. THE TYPE OF ERROR TO BE MEASURED AND THE MEASUREMENT MODE MUST THEN BE SELECTED. IF THE ERROR RATE MODE IS SELECTED BY PUSHING THE APPROPRIATE PUSHBUTTON (10^{-4}, 10^{-5}, 10^{-6}, 10^{-7}, 10^{-8}), THE ERROR INDICATION WILL APPEAR ON THE COUNT DISPLAY AT THE RATE SELECTED. IF TOTAL ERRORS IS SELECTED, INDIVIDUAL ERRORS ARE RECORDED UP TO 99,999 (WITH AN OVERFLOW INDICATION). THE ERROR-SEC SELECTION WILL COUNT SYNCHRONOUS ERRORED SECONDS UP TO 99,999 (WITH AN OVERFLOW INDICATION). ERROR RATE, TOTAL, AND ERROR-SECOND MEASUREMENTS ARE DONE SIMULTANEOUSLY. THESE SWITCHES MAY BE CHANGED ANY TIME DURING THE TEST TO READ CURRENT ERROR STATUS.

THE TOTAL AND ERROR-SEC PUSHBUTTONS ARE USED IN CONJUNCTION WITH THE UNTIMED/TIMED TOGGLE SWITCH AND THE TIME INTERVAL COUNTER.

IN THE UNTIMED POSITION, THE START/RESET PUSHBUTTON IS MOMENTARILY PUSHED TO START THE TEST. PUSHING THE STOP PUSHBUTTON WILL TERMINATE THE MEASUREMENT PERIOD.

IN THE TIMED POSITION, THE SPECIFIED TIME IS SELECTED ON THE TIME INTERVAL COUNTER (1 MINUTE TO 999 HRS., 99 MIN.), AND THE START/RESET PUSHBUTTON IS PUSHED TO INITIATE THE MEASUREMENT PERIOD. THE MEASUREMENT WILL TERMINATE AT EITHER THE END OF THE SELECTED TIME PERIOD OR BY PUSHING THE STOP PUSHBUTTON. THE REMAINING TIME IN ANY MEASUREMENT PERIOD MAY BE SEEN ON THE COUNTER DISPLAY BY MOMENTARILY PUSHING THE UNTIMED/TIMED/TIME TO GO TOGGLE SWITCH TO THE TIME TO GO POSITION. THIS ACTION WILL NOT EFFECT THE MEASUREMENT PERIOD.

DURING THE OPERATION OF THE TEST SET, THE INDICATORS ON THE FRONT PANEL WILL SHOW THE STATUS AND CONDITION OF THE INPUT BEING TESTED. IF ANY INDICATOR LAMP ON THE COUNTER IS SUSPECTED OF FAILURE, PUSH THE HISTORY RESET/LED TEST PUSHBUTTON.

Note also, however, that this action will extinguish any of the history lamps if they were previously illuminated. Refer to Table 3-1 for the definition and location of all indicators.

A test of the receiver can be made by selecting a specific rate (DS1, DS1C, or DS2) and applying an input signal from the matching transmitter at that rate.

The Test Set can also be used to test the Automatic Protection Switch operation in conjunction with the compatible S5102 Transmitter. Data that are received at the INPUT connector of the Receiver Test Set also appear at the APS OUT connector on the rear of the Receiver Test Set. The data from this connector can be coupled to the APS IN connector at the rear of the Transmitter Test Set. This will route the received signal directly through the output amplifiers in the Transmitter Test Set for retransmission through the communications equipment and back to the Receiver Test Set. (Refer to Fig. 3-2).

SHUTDOWN PROCEDURE

The Test Set requires no specific shutdown procedure. Once the signal plug has been removed, the POWER pushbutton/Indicator may be pushed, the power plug removed, and the Test Set cover replaced with the power cord stored in the cover.

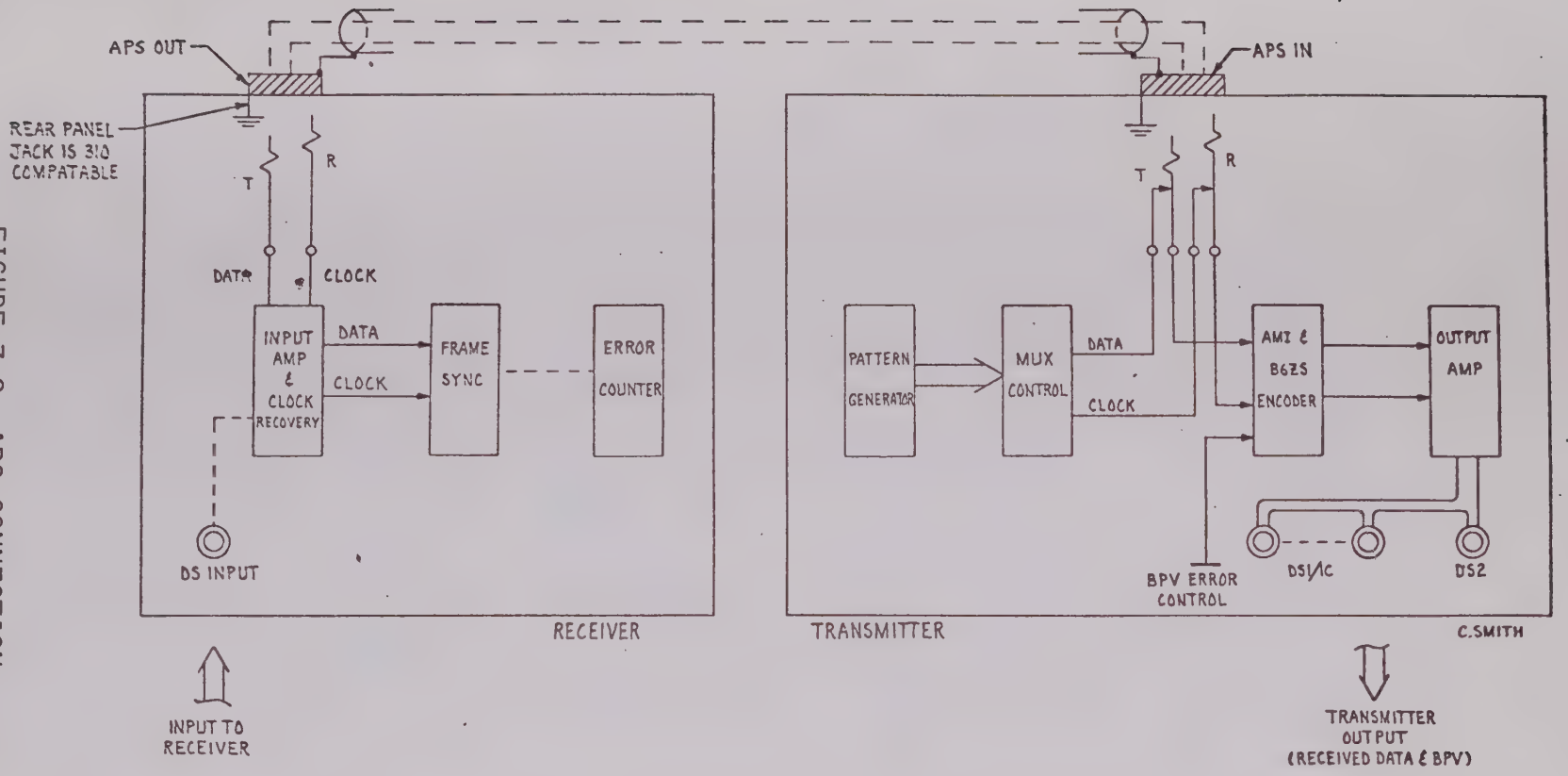


FIGURE 3-2 APS CONNECTION

SECTION 4
PRINCIPLES OF OPERATION

INTRODUCTION

This section contains the theory of operation for the S5102 Error Rate Test Set (Receiver) and is discussed at two levels. The first level is an overall description referenced to the functional block diagram (Fig. 6-1). The second level of theory is based on the schematic and component location diagrams, Figures 6-2 through 6-12. Table 4-1 lists the Receiver specifications.

OVERALL FUNCTIONAL DESCRIPTION

The seven major functional areas of the Receiver Test Set are illustrated in Figure 6-1, and the general theory of operation is described in the following paragraphs.

INPUT AMPLIFIER/CLOCK RECOVERY

The input Amplifier/Clock/Recovery PCB provides the input signal conditioning, amplification, format conversion (Bipolar to NRZ, and clock recovery for the three DS rates covered by this test set. In addition to these functions, the incoming data are checked for line code violations, excessive strings of zeros, while the demultiplexed channel data are checked for an all ONE's content.

TABLE 4-1

RECEIVER SPECIFICATIONS

T-1004

	DS1	DS1C	DS2
INPUT			
FREQUENCY	CLOCK RECOVERED FROM INPUT SIGNAL		
CODE	AMI	AMI	B6ZS
LEVEL	±3.0V NOM. PLUS UP TO 750' ABAM CABLE PLUS UP TO 20DB ATTENUATION	±3.0V NOM. PLUS UP TO 655' ABAM CABLE PLUS UP TO 20DB ATTENUATION	HI: ±2.1V NOM. DSX/LO; ±2.1V NOM PLUS UP TO 2100' ABAM CABLE PLUS UP TO 6DB ATTENUATION, OR ±2.1V NOM. PLUS UP TO 1000' ABAM CABLE PLUS UP TO 40DB ATTENUATION.
INTERFACE	ONE FRONT-PANEL CONNECTOR. (WECO 310 PLUG-COMPATIBLE)		
IMPEDANCE	110 OHMS, BALANCED.		
RETURN LOSS	>26DB FOR FREQUENCY RANGE 0.3 TO 12.6MHZ		
CHANNEL			
SELECT	1	1,2	1,2,3,4
INVALID SELECTION	NUMERICAL DISPLAY WILL FLASH.		
ERROR MEASUREMENT			
BIPOLAR	CODE VIOLATIONS OCCURRING ON DS1, DS1C, OR DS2 INPUT DATA ON EITHER LIVE TRAFFIC OR TEST PATTERN.		
BIT	COMPARISON OF THE RECEIVER'S DS1 PSEUDORANDOM GENERATOR AND THE RECEIVED DS1 CHANNEL UNDER TEST.		
ERROR COUNTERS (SIMULTANEOUS)			
TOTAL ERRORS	COUNTS INDIVIDUAL ERRORS UP TO 99,999. OVERFLOW INDICATION.		
ERROR SECONDS	COUNTS SYNCHRONOUS ERRORED SECONDS UP TO 99,999. OVERFLOW INDICATION. MEASUREMENT IS DETERMINED BY OCCURRENCE OF A TOTALIZED ERROR WHICH THEN TRIGGERS A PRECISION ONE SECOND PERIOD. AT THE END OF THIS PERIOD THE NEXT ERROR WILL GENERATE THE NEXT ERRORED SECOND.		
ERROR RATE	THREE DIGIT COUNTER WITH EXPONENTIAL RANGE SELECTED MANUALLY VIA FRONT-PANEL INTERLOCKING SWITCHES. RANGE 10^{-4} TO 10^{-8} FOR INTEGER VALUES OF THE EXPONENT. GATING: DISPLAY IS UPDATED AT THE END OF EACH TIME PERIOD FROM THE TABLE BELOW.		

RANGE SELECTED	BIPOLAR DS1	DS1C	DS2	BIT DS1	BIT DS1C	BIT DS2
10^{-4}	1	1	1	1	1	1
10^{-5}	1	1	1	1	1	1
10^{-6}	1	1	1	1	1	1
10^{-7}	6.5	3.2	1.6	6.5	6.5	6.5
10^{-8}	65	32	16	65	65	65

TABLE 4-1

RECEIVER SPECIFICATIONS (CONTINUED)

DISPLAY	
TYPE	LED
DIGITS	5 WITH OVERFLOW
TIMER	
CONTROLS	5-DIGIT THUMBWHEEL-TIME INTERVAL; 2-PUSHBUTTON MEARUREMENT START AND STOP; 3-POSITION TOGGLE MODE SWITCH.
TIME RANGE	999 HRS., 99 MIN.
MODE	UNTIMED: TOTAL AND ERROR-SEC COUNTS MADE CONTINUOUSLY WITHOUT REGARD TO TIME MEASUREMENT CONTROLLED BY START/RESET. TIMED: TOTAL AND ERROR-SEC COUNTS BEGIN WITH START, TIME ENTERED AS SET ON THUMBWHEEL SWITCHES DETERMINES TEST DURATION. TIME TO GO: DISPLAYS TIME REMAINING DURING A TIMED TEST. NO EFFECT ON MEASUREMENT.
INDICATORS	
OUT OF FRAME DEMUX ON (DS1C OR DS2)	LED (RED) INDICATES DETECTION OF LOST FRAME CONDITION, LATCHING LED (AMBER) INDICATES PAST DETECTION OF FRAME LOSS, AND REMAINS ON UNTIL RESET BY FRONT-PANEL PUSHBUTTON.
EXCESS ZEROS	LED (RED) INDICATES DETECTION OF EXCESSIVE NUMBER OF CONSECUTIVE ZEROS IN INCOMING DATA, MINIMUM NUMBER OF ZEROS REQUIRED TO TURN ON LED IS; DS1:16, DS1C:34, DS2:6, LATCHING (AMBER) LED INDICATES PAST DETECTION OF EXCESS ZEROS AND REMAINS ON UNTIL RESET BY FRONT-PANEL PUSHBUTTON.
NO SYNC	LED (RED) INDICATES DETECTION OF LOST PR-SYNC CONDITION, LATCHING LED (RED) INDICATES PAST DETECTION OF LOST PR-SYNC, AND REMAINS ON UNTIL RESET BY FRONT-PANEL PUSHBUTTON.
TEST IN PROCESS	INDICATES ON FOR DURATION OF TIMED TEST, FLASHES OFF MOMENTARILY ON RATE MEASUREMENTS WHEN NEW DATA ARE LOADED TO DISPLAY.
ALL ONES	INDICATES ON WHENDEMULTIPLEXED DS1C CHANNEL 2 OR RECEIVED DS1 DATA ARE ALL ONES.
X-BIT	INDICATES ON FOR X BIT = LOGIC 0. INDICATES OFF FOR X-BIT = LOGIC 1. (DS1C AND DS2 ONLY, DEMUX ON)
LOST POWER	INDICATES ON FOLLOWING RESTORATION OF 60HZ POWER AFTER A LOW-LINE OR POWER-FAIL CONDITION UNTIL RESET BY FRONT-PANEL PUSHBUTTON.

TABLE 4-1

RECEIVER SPECIFICATIONS (CONTINUED)

AUXILIARY FUNCTIONS	
APS TRANSMITTER OUTPUT	REAR-PANEL CONNECTOR (WECO 310 PLUG-COMPATIBLE), WHICH FACILITATES THE TESTING OF CERTAIN TYPES OF T1, SPAN SYSTEM AUTOMATIC PROTECTING SWITCHES. TO BE USED IN CONJUNCTION WITH TRANSMITTER REAR-PANEL INPUT ONLY. INCLUDES SIGNAL CLOCK AND DATA.
LED TEST/HISTORY RESET	WHEN ACTIVATED ILLUMINATES ALL LEDS AND RESETS THE HISTORY INDICATORS.
MONITOR JACKS	
RECOVERED CLOCK	FROM DATA INPUT.
M-FRAME SYNC PULSE	ONCE PER M-FRAME (DS1C AND DS2)
PR-SYNC PULSE	ONCE PER SEQUENCE.
COUNT	ONE PULSE PER ERROR OR ERRORED SECOND DEPENDING UPON SELECTED DISPLAY MODE.
BIT ERROR	ONE PULSE EACH BIT ERROR DETECTED.
TYPE	REAR-PANEL BNC 75 OHMS.
LEVEL	2.5V INTO 75 OHMS FROM 75 OHM SOURCE.
GENERAL	
POWER	115 VAC ±10% 50 TO 400Hz <40 VA.
SIZE	0.25H x 13.0W x 11.75D.
WEIGHT	16 LBS (7.3KG).
ACCESSORIES	POWER CABLE, INSTRUCTION MANUAL, PROTECTIVE COVER.

FRAME SYNC

THE FUNCTION OF THE FRAME SYNC IS TO SYNCHRONIZE THE RECEIVER WITH THE INCOMING DS1C OR DS2 DATA STREAM SO THAT THE CONTROL BITS (MFC) AND THE STUFFING BITS CAN BE REMOVED FROM THE DATA (INFORMATION BITS). DURING DS1 OPERATION AND THE DEMUX OFF MODE, THE CIRCUITRY DOES NOT SYNCHRONIZE OR MODIFY THE INCOMING CLOCK AND DATA, BUT MERELY PASSES THEM ON TO THE DEMULTIPLEXER BOARD.

DEMULTIPLEXER

THE FUNCTION OF THE DEMULTIPLEXER IS TO SEPARATE THE INCOMING DS RATE DATA INTO THE ORIGINAL DS1 DATA PATTERNS THAT WERE MULTIPLEXED TOGETHER BY THE TRANSMITTER. THE DEMULTIPLEXING IS DONE ONLY AT THE DS1C AND DS2 RATES (DEMUX ON). UPON INSTRUCTION FROM THE C-BITS, THE STUFFED BITS LOCATED WITHIN THE DATA FIELD ARE REMOVED.

AN OVERVIEW OF WHAT OCCURS DURING THE DEMULTIPLEX OPERATION FOR EACH CHANNEL SELECTION IS LISTED BELOW. (REFER TO TABLE 3-1).

A. CHANNEL SELECT 1

1. DS1.....REQUIRED SELECTION FOR DS1.
2. DS1C.....CAUSES DEMUX CLOCK TO ALIGN WITH DATA BITS ASSOCIATED WITH CHANNEL 1 INFORMATION BITS.

B. CHANNEL SELECT 2

1. DS1-----Illegal selection.

2. DS1C-------Causes Demux clock to align with data bits associated with Channel 2 information bits. Inverts data prior to sampling.

C. CHANNEL SELECT 3

1. DS1/DS1C-----Illegal selection.

2. DS2-----Causes Demux clock to align with data bits associated with Channel 3 information bits.

D. CHANNEL SELECT 4

1. DS1/DS1C-----Illegal selection.

2. DS2-----Causes Demux clock to align with data bits associated with Channel 4 information bits. Inverts data prior to sampling.

PR Sync

The purpose of the PR Sync function is to check for incoming bit errors on the received demultiplexed data stream. The incoming data are checked against a locally generated test pattern which is identical to the basic pseudorandom sequence that is generated within the transmitter. This test pattern is synchronized with the incoming data by a feed-forward

TECHNIQUE. ONCE SYNCHRONIZED, THE INCOMING DATA ARE COMPARED ON A BIT-BY-BIT BASIS WITH THE LOCALLY GENERATED TEST PATTERN.

ERROR ACCUMULATOR

THE ERROR ACCUMULATOR CONSISTS OF THREE INDEPENDENT COUNTERS THAT ARE USED TO MEASURE SIMULTANEOUS ERROR-RATE, TOTAL ERRORS, AND TOTAL ERROR-SECONDS FOR EITHER BIT ERRORS OR BIPOLAR VIOLATIONS. THE CONTENTS OF EACH COUNTER ARE DISPLAYED ON A 5-DIGIT COMMON DISPLAY (3 DIGITS FOR ERROR-RATE). THE SELECTION OF WHICH COUNTER'S CONTENTS IS BEING DISPLAYED CAN BE CHANGED AT ANY TIME DURING A MEASUREMENT PERIOD WITHOUT INTERRUPTING THE COUNTING PROCESS. THE TYPE OF ERROR BEING MEASURED (BIT OR BIPOLAR) CANNOT BE CHANGED ONCE A MEASUREMENT HAS BEEN INITIATED WITHOUT INVALIDATING THE DATA ACCUMULATED.

TIMER

THE TIMER CONTAINS THE LOGIC FOR THE TEST TIME INTERVAL OSCILLATOR AND COUNTER, THE ERROR COUNT AND TIME REMAINING DISPLAY MULTIPLEXER, AND THE LOST POWER MONITOR.

DISPLAY

THE DISPLAY IS A FIVE DIGIT LATCHING DISPLAY AND LED INDICATOR FOR DISPLAYING BOTH CURRENT AND HISTORY STATUS.

DETAILED SYSTEM OPERATION

THE FOLLOWING PARAGRAPHS CONTAIN A STEP-BY-STEP FUNCTIONAL

ANALYSIS OF THE TEST SET. REFER TO FIGURE 6-1 FOR THE OVERALL FUNCTIONAL DESCRIPTION OF THE TEST SET. REFERENCE IS ALSO MADE THROUGHOUT THIS SECTION TO OTHER SPECIFIC SCHEMATIC DIAGRAMS, COMPONENT LOCATIONS, AND INTERCONNECTION DIAGRAMS THAT ARE LISTED IN SECTION 6.

REFERENCES TO INDIVIDUAL CIRCUIT COMPONENTS IN SCHEMATIC DIAGRAMS ARE MADE BY USING AN ALPHANUMERIC DESIGNATION FOLLOWED BY PIN NUMBER, WHERE APPLICABLE. A TEXT REFERENCE TO U24-6, FOR EXAMPLE, INDICATES PIN 6 OF THE LOGIC ELEMENT U24.

INPUT AMPLIFIER CLOCK RECOVERY THEORY OF OPERATION

THE INPUT TO THIS PCB IS ATTENUATED BY A RESISTIVE PAD LOCATED ON THE INPUT JACK TO PREVENT THE AMPLIFIER FROM BECOMING OVERLOADED. THE INCOMING BIPOLAR DATA ARE CONVERTED FROM A BALANCED SIGNAL INTO AN UNBALANCED SIGNAL BY THE TRANSFORMER (T1). THE SIGNAL IS THEN BUFFERED BY Q1 BEFORE BEING PASSED THROUGH A LOW-PASS FILTER (L2/L3, C4/C5/C6).

THE DS2 CROSS-CONNECT (DSX) AND THE LOW LEVEL (LO) SIGNALS MUST BE EQUALIZED BY THE BRIDGED-T NETWORK. ALL OTHER SIGNAL LEVELS AND RATES ARE UNEQUALIZED BUT ATTENUATED BY THE T-PAD ATTENUATOR (R10, R11, AND R12).

THE CONDITIONED BIPOLAR SIGNAL IS AMPLIFIED BY A TWO-STAGE WIDEBAND AMPLIFIER WHICH HAS OVER 40DB OF DYNAMIC RANGE. THE GAIN OF THE AMPLIFIERS IS CONTROLLED BY THE AGC (AUTOMATIC GAIN CONTROL) VOLTAGE DEVELOPED BY A PEAK DETECTOR/INTEGRATOR CIRCUIT AT THE OUTPUT OF THE SECOND AMPLIFIER.

THE AMPLITUDE OF THE OUTPUT SIGNAL IS SET BY THE REFERENCE VOLTAGE APPLIED TO THE NON-INVERTING INPUTS OF THE OP-AMP AT C2. THE SUPPLY VOLTAGE USED BY THE REFERENCE AMPLIFIER (Q3) AND THE PEAK-DETECTOR BUFFER (Q4) IS DEVELOPED BY A TEMPERATURE COMPENSATED ZENER DIODE CR1.

THE FINAL OUTPUT STAGE PROVIDES BOTH DATA AND THE COMPLEMENT OF THE DATA. THESE BIPOLAR DATA ARE LEVEL SLICED BY THE LINE RECEIVER LOCATED AT D4. THE RESULTING RZ DATA AT D4-15 AND D4-3 ARE LEVEL TRANSLATED, BY THE TRANSISTOR PAIRS Q5, Q7, Q6, AND Q8 INTO TTL LEVELS.

THE RZ DATA ARE CONVERTED INTO NRZ BY CLOCKING THE DATA INTO THE REGISTER LOCATED AT D7. THE P AND N RAILS ARE CHECKED FOR VIOLATIONS BY THE CIRCUIT AT F9 AND F8. THIS CIRCUIT PRODUCES AN OUTPUT THAT IS STORED IN REGISTER D9 EACH TIME THE OCCURRENCE OF THE P AND N RAILS FAILS TO ALTERNATE. DURING DS1 AND DS1C RATES, THESE ERRORS ARE CLOCKED OUT OF THE REGISTER AND ARE GATED TO THE ERROR COUNTER AS BPV (BIPOLAR VIOLATIONS).

THE DS2 SIGNAL IS HANDLED SLIGHTLY DIFFERENTLY IN THAT THE P AND N RAILS ARE EXAMINED NOT ONLY FOR BIPOLAR VIOLATIONS BUT FOR THE OCCURRENCE OF A B6ZS CODE. THE CRITERIA FOR CODE IDENTIFICATION ARE THE DETECTED OCCURRENCE OF THE PATTERN - OVBOBV, WHERE O IS A LOGICAL ZERO DATA BIT, V IS A VIOLATION DATA BIT, AND B IS A NON-VIOLATION LOGICAL ONE DATA BIT. THE INCOMING DATA ARE PASSED THROUGH A SHIFT REGISTER (D8) WHICH CHECKS THE DATA FOR THE 011011 CONDITION, WHILE AT THE SAME TIME REGISTER D9 IS RECORDING ANY DETECTED VIOLATION (010010). IF THESE TWO CONDITIONS MATCH, AS DETECTED BY B9-9 THEN THE VIOLATION REGISTER AND THE DATA REGISTER (D9 AND D7) ARE CLEARED.

THE SECONDARY FUNCTION OF THE REGISTER AT D8 IS TO DETECT THE OCCURRENCE OF SIX ZEROS IN THE INCOMING DS2 DATA. THE DETECTION OF SIX ZEROS (B7-8) IS GATED TO THE ONE-SHOT (A6) WHICH, WHEN TRIGGERED, PROVIDES THE SIGNALS USED TO LIGHT THE EXCESS ZEROS LED.

THE DS1 AND DS1C EXCESSIVE ZERO DETECTOR IS LOCATED AT D5, B5, AND A5. THIS CIRCUIT CONTAINS THE NUMBER OF CONSECUTIVE ZEROS IN THE DATA PATTERN, EACH LOGICAL 1 RESETS THE COUNTERS. THE MINIMUM NUMBER OF CONSECUTIVE ZEROS REQUIRED TO ACTIVATE THE EXCESS ZEROS LED IS 16 FOR DS1 AND 34 FOR DS1C. THE ALL ONES DETECTOR IS LOCATED AT A6. THIS ONE-SHOT IS KEPT IN A TRIGGER STATE (A6-12 LOGICAL 1) BY THE RZ PULSES RECEIVED FROM THE DEMULTIPLEXER (PC7). A PULSE OCCURS EACH TIME A LOGIC "0" IS DETECTED IN THE DEMULTIPLEXED DATA PATTERN OF THE DS1C/DS2 CHANNEL SELECTED. SINCE NO DEMULTIPLEXING OCCURS ON A DS1 SIGNAL, THE ALL ONES CONDITION IS CHECKED ON THE RECEIVED DS1 PATTERN. IF A SERIES OF LOGICAL ONES IS DETECTED THAT EXCEED THE TIME CONSTANT OF THE ONE-SHOT (1000 DATA BITS), THE ONE-SHOT WILL TIME-OUT CAUSING THE ALL ONES LED TO LIGHT.

THE TIMING INFORMATION IS EXTRACTED FROM THE RZ DATA BY THE PHASE-LOCKED LOOP. THE CENTER OPERATING (FREE RUNNING) FREQUENCIES ARE ADJUSTABLE BY C47, C49, AND C51.

INPUT/AMPLIFIER CLOCK RECOVERY CIRCUIT - INPUT/OUTPUT SIGNAL DESIGNATIONS

DS1(L) --- FRONT-PANEL CONTROL SIGNAL (ACTIVE WHEN GROUNDED). CONTROLS THE SELECTION OF DS1 FUNCTIONS.

DS1C (L)---SAME AS ABOVE EXCEPT CONTROLS DS1C FUNCTIONS.

DS2(L)---SAME AS ABOVE EXCEPT CONTROLS DS2 FUNCTIONS.

DSX-2(H)---FRONT-PANEL CONTROL SIGNAL (ACTIVE WHEN OPEN). CAUSES THE INPUT SIGNAL TO BE CONDITIONED BY THE LINE EQUALIZER.

ERROR-SEC (L)---FRONT-PANEL CONTROL SIGNAL (ACTIVE WHEN GROUNDED). ENABLES THE BPV LOGIC TO OUTPUT ERROR PULSES DURING A LOST DATA CONDITION (EXCESSIVE ZEROS).

BIPOLAR INPUT---BALANCED 110 OHM INPUT PORT.

DATA--- NRZ OUTPUT DATA.

BPV---RZ OUTPUT PULSE THAT OCCURS WHEN A BIPOLAR VIOLATION IS DETECTED. IF THE BPV WAS DUE TO THE B6ZS CODING, NO OUTPUT RESULTS.

DS CLOCK--- BUFFERED RECOVERED CLOCK OUTPUT.

DS CLOCK-1--- SAME AS ABOVE.

EXCESS ZEROS--- LED DRIVER OUTPUT. INDICATES THAT AT LEAST 16, 34, OR 6 ZEROS WERE DETECTED ON A DS1, DS1C, OR DS2 INPUT SIGNAL, RESPECTIVELY.

LOST DATA --- OUTPUT SIGNAL USED BY DISPLAY PCB TO LATCH THE CONDITION OF EXCESS ZEROS.

ALL ONES --- LED DRIVER OUTPUT. INDICATES THAT THE CHANNEL SELECTED FOR DEMULTIPLEXING CONTAINED A SERIES OF LOGICAL ONES WHICH EXCEEDED THE NOMINAL THRESHOLD OF 1,000 BITS.

ONES DATA --- INPUT DATA FROM THE DEMUX PCB. USED TO DRIVE THE ALL ONES DETECTOR LOGIC.

TP-1 --- BIPOLAR VIOLATION PULSE OUTPUT.

TP-3 --- RECOVERED DS RATE CLOCK.

TP-4 --- AMPLIFIED BIPOLAR DATA FOR N RAIL SLICING.

TP-5 --- SLICING THRESHOLD VOLTAGE.

TP-6 --- AMPLIFIED BIPOLAR DATA FOR P RAIL SLICING.

TP-8 --- AGC LOOP VOLTAGE.

Frame Sync Theory of Operation

The incoming data are sampled each 53rd or 49th time slot (DS1C/DS2, respectively) and the results are compared at U26 with a locally generated MFC bit pattern (U15). The results of the comparison (correct/error) are separated into individual groups of F bits (U42-13), U34-8), M-bits (U16-8), and C-bits (U34-6).

The correct F-bit decisions are counted at U20 with the F-Frame Valid (U37-5, TP3) being achieved if nine or more consecutive F-bits are found correctly. If three F-bit errors are found between M4 time slots, F-Frame Valid is cleared and a bit slip is requested by U38-5. This bit slip causes the next 53rd or 49th sample to occur one time slot later than it would have normally occurred. Once the F-Frame has been found successfully, the M-bits are examined for their correct sequence. If no M-bit errors are detected in the major frame following frame alignment, then M-frame is deemed valid (U18-5). If an M-bit error is detected, then the signal Trig M-CTR is generated at U42-1. This signal will advance the local M-sequence generator at U33 and U24 by one step. The M-bits are again compared during the next major frame. If no further steps are required, the M-frame is deemed valid and the OUT OF FRAME led turns off.

Once the frame sync has been achieved (for both F and M), two conditions will cause an out of frame condition. The first is if three or more F-bit errors occur between M4 time slots. The second is if three or more cumulative M-bit errors occur in three consecutive major frames. The M-bit errors that occur during a major frame are sequentially stored into one of the three registers at U12, U10, or U11. One of the three

REGISTERS WILL STORE THE M-BIT ERRORS THAT ARE OCCURRING DURING THE PRESENT MAJOR FRAME, WHILE THE OTHER TWO STORE THE RESULTS OF THE PRECEEDING TWO FRAMES. THE LOGIC AT U17, U19, AND U28 IS MONITORING THE QUANTITY OF M-BIT ERRORS STORED AND, IF THREE ERRORS ARE DETECTED, THE M-FRAME VALID U18-5 IS CLEARED.

THE LOCAL MFC BIT GENERATOR CONSISTS OF AN M-BIT GENERATOR AND AN F AND C BIT GENERATOR. THE M-BIT GENERATOR IS FORMED BY SEQUENCING A DATA SELECTOR (U24) WHOSE INPUT IS A FIXED 0110 PATTERN. THE DATA SELECTOR IS CONTROLLED BY THE STATE OF THE 2-BIT COUNTER (U33) WHICH IS INCREMENTED EACH SUB-FRAME DURING THE F1 TIME SLOT. THE RESULTING M-BIT PATTERN IS USED AS AN INPUT TO THE SECOND DATA SELECTOR (U15). THE OUTPUT OF THIS SELECTOR IS THE FINAL OVERHEAD PATTERN AND IS CONTROLLED BY THE DECODING OF THE COUNTER AT U5, U6, AND U14. AS WERE THE M-BITS, THE F AND C BITS ARE FIXED INPUTS TO THE SECOND SELECTOR WITH SEQUENCING OCCURRING DURING THE 53RD OR 49TH TIME SLOT FOR DS1C AND DS2, RESPECTIVELY.

FRAME SYNC CIRCUIT INPUT/OUTPUT SIGNAL DESIGNATIONS

DS1(L) --- FRONT-PANEL CONTROL LINE THAT IS ACTIVE (GROUND) WHEN THE DS1 INPUT SWITCH IS PUSHED.

DS1C(L) --- SAME AS ABOVE EXCEPT ACTIVE WHEN DS1C IS SELECTED.

DS2(L)--- SAME AS ABOVE EXCEPT ACTIVE WHEN DS2 IS SELECTED.

DS CLOCK --- RECOVERED DS CLOCK FROM THE INPUT/CLOCK RECOVERY PCB.

DATA --- NRZ DATA INPUT. THESE DATA, IF DS1C OR DS2, CONTAIN THE CONTROL BITS AND STUFF BITS.

GAPPED CLOCK --- CLOCK OUTPUT THAT CONTAINS A GAP (ABSENCE OF A PULSE) EACH 53RD OR 49TH TIME SLOT FOR DS1C/DS2, RESPECTIVELY. SAME AS DS CLOCK IF DS1 IS SELECTED.

DATA-1 --- NRZ DATA OUTPUT. THESE DATA, IF DS1C OR DS2, HAVE HAD THE CONTROL BITS (MFC) REMOVED BUT STILL CONTAIN THE STUFF BITS. SAME AS DATA IF DS1 IS SELECTED.

LOST FRAME --- OUTPUT THAT DRIVES THE FRONT-PANEL DISPLAY LATCHING CIRCUIT WHICH DENOTES THE OCCURRENCE OF AN OUT OF FRAME CONDITION.

OUT OF FRAME --- OUTPUT THAT DRIVES FRONT-PANEL LED LOSS OF FRAME ALIGNMENT (DS1C/DS2).

M4(H) --- OUTPUT SIGNAL THAT MARKS THE 4TH M-BIT LOCATION. THIS SIGNAL IS USED BY THE DEMUX PCB (DS1C/DS2).

M1(H) --- SAME AS ABOVE EXCEPT MARKS 1ST M-BIT LOCATION (DS1C/DS2).

X-BIT --- OUTPUT THAT DRIVES X-BIT LED. DECODED LOGIC LEVEL OF THE M4 BIT (DS1C/DS2).

C=1(H) --- OUTPUT SIGNAL THAT IS THE DECODED LOGIC STATE OF THE C-BITS (DS1C/DS2).

F1(H) --- OUTPUT SIGNAL THAT MARKS THE LOCATION OF THE F1 BITS (DS1C/DS2).

Demultiplexer Theory of Operation

The gapped clock input signal is converted into the Demux clock (DS1C/DS2) by either dividing by two or by four for DS1C and DS2, respectively. In order that the resulting clock aligns with the desired channel bits, the division process is synchronized by the enable signal generated at U5-8. The counters (U2) start the division process on either the first, second, third, or fourth clock following an F1 bit. The selection is controlled by the channel selection input (CH1 through CH4). The Demux clock will have the frequency shown below.

DS1-----1544.000 kHz

DS1C----1546.264 kHz

DS2-----1545.796 kHz

The above frequencies can be calculated by using the following mathematical expression.

Demux Clock = Gapped Clock ÷ number of channels in DS format

Example: DS1C

$$\text{Gapped clock} = \text{DS clock rate} \times \frac{\text{No. of data bits between OH bits}}{\text{OH bit spacing}}$$

$$= 3142.00 \times \frac{52}{53}$$

$$= 3092.5283 \text{ kHz}$$

THE NUMBER OF DS1 CHANNELS THAT ARE MULTIPLEXED IN FORMING A DS1C SIGNAL IS 2.

THEREFORE, DEMUX CLOCK = 3092.5283 ÷

= 1546.264 KHZ

THE INCOMING DS RATE DATA ARE PROCESSED BY THE LOGIC AT U22 AND U23. EVEN CHANNEL SELECTIONS CAUSE THE DATA TO BE INVERTED (U23-4 LOGICAL 1) PROVIDED THE CHANNEL SELECTED IS LEGAL. IF DS1C DATA ARE BEING PROCESSED, PRIOR TO ANY INVERSION THE DATA ARE DESCRAMBLED IN A SINGLE STAGE DESCRAMBLER CIRCUIT (U22 AND U23). THE OUTPUT IS THE MODULO-2 SUM NEXT BIT AND THE LAST BIT.

THESE PROCESSED DATA ARE SAMPLED AT U22-12 BY THE PN CLOCK. THIS CLOCK IS THE DEMUX CLOCK THAT HAS BEEN GAPPED (PULSES REMOVED) AT THE TIME SLOTS WHICH COINCIDE WITH STUFF BITS. THE SAMPLED OUTPUT (U22-9) CONSISTS ONLY OF THE ORIGINAL PSEUDORANDOM TEST PATTERN WITH A BIT RATE OF 1544 KHZ.

THE DESTUFFING LOGIC MONITORS THE C=1, F1, AND M4 CONTROL LINES. IF WITHIN ANY SUB-FRAME, TWO OF THE THREE C-BITS ARE FOUND TO BE LOGICAL ONES, A DESTUFF REQUEST (U7-8) IS GENERATED IN SUCH A WAY THAT THE APPROPRIATE CLOCK PULSE IS REMOVED FROM THE PN CLOCK SIGNAL (U17 AND U3).

Demultiplexer Input/Output Signal Designations

DS1----- Front-panel switch selection, active when ground. Enables DS1 function.

DS1C --- Same as above except enables DS1C functions.

DS2 --- Same as above except enables DS2 functions.

CH1 --- Front-panel switch selection, active when ground. Selects Channel 1 data for sampling.

CH2 --- Same as CH1 except selects Channel 2.

CH3 --- Same as CH1 except selects Channel 3.

CH4 --- Same as CH1 except selects Channel 4.

Gapped Clock --- Clock received from Frame sync PCB that has been gapped at the time slots, which coincide with the OH bits in the DS1C and DS2 data streams.

DS Data --- Data from the Frame sync PCB that have had the control bits (OH bit) removed.

M4 --- Pulse input from the Frame sync PCB that mark the occurrence of the 4th M-bit in each major frame.

F1 --- Pulse input from the Frame sync PCB that marks the occurrence of the F1 bit in each sub-frame.

C=1 --- Pulse input from the Frame sync PCB that indicates that a C-bit was found to be a logical 1. If two of the three

C-BITS IN A SUB-FRAME ARE FOUND TO BE LOGICAL 1'S, THEN A DE-STUFFING OPERATION IS INITIATED.

M1 --- PULSE INPUT FROM THE FRAME SYNC PCB THAT MARKS THE OCCURRENCE OF THE 1ST M-BIT IN EACH MAJOR FRAME USED TO GENERATE M-BIT SYNC.

M-BIT SYNC --- M1 OUTPUT SIGNAL (AVAILABLE AT REAR PANEL).

DEMUX DATA --- DEMULTIPLEXED AND DESTUFFED DATA. THESE ARE DATA THAT ARE CHECKED FOR BIT ERRORS.

ONES DATA --- EACH TIME THE DEMUX DATA CONTAIN A ZERO DATA BIT, U24-6 IS PULSED LOW. THIS SIGNAL IS USED BY THE ALL ONES DATA DETECTOR LOCATED AT THE INPUT AMPLIFIER/CLOCK RECOVERY PCB.

PN CLOCK --- CLOCK USED IN SAMPLING THE INCOMING DS DATA. THE CLOCK HAS AN AVERAGE RATE OF 1544 KHZ.

PR SYNC THEORY OF OPERATION

THIS BOARD CAN BE DIVIDED INTO TWO LOGIC FUNCTIONS. THE FIRST OF WHICH IS A PSEUDORANDOM PATTERN GENERATOR AND THE SECOND IS A BIT SYNCHRONIZER. THE PSEUDORANDOM PATTERN GENERATOR CONSISTS OF A 20 STAGE SHIFT REGISTER WITH EXCLUSIVE-OR FEEDBACK TAPS AT THE 17TH AND 20TH STAGES. DURING BIT SYNCHRONIZATION THE FEEDFORWARD DATA ARE FED THROUGH GATES U24 INTO THE INPUT OF THE 18TH STAGE OF THE PATTERN GENERATOR. THE OUTPUT OF THE PSEUDORANDOM GENERATOR, ONCE SYNCHRONIZATION HAS BEEN ACHIEVED, IS TAKEN FROM THE 17TH STAGE OUTPUT. THE OUTPUT IS FORCED TO A LOGICAL "1" (U22-3) WHENEVER THE NEXT 14 BITS OF THE SEQUENCE ARE A LOGICAL "0" (MUX ON ONLY).

THIS MODIFICATION RESULTS IN A 14 ZERO CONSTRAINT PSEUDORANDOM SEQUENCE AND IS IDENTICAL TO THE ONE GENERATED BY THE TRANSMITTER. THIS MODIFIED SEQUENCE IS COMPARED WITH THE INCOMING DEMULTIPLEXED BIT STREAM BY THE EXCLUSIVE-OR GATE AT U17. DURING THE DEMUX OFF MODE, THE DATA ARE NOT MODIFIED BY THE 14 ZERO CONSTRAINT LOGIC.

THE RESULT OF THIS COMPARISON IS STORED BY THE FLIP-FLOP AT U26. IF AN INCORRECT COMPARISON IS RECORDED, THE OUTPUT OF THE FLIP-FLOP IS GATED AGAINST A CLOCK AT U25 RESULTING IN THE SIGNAL BIT ERROR. BIT SYNCHRONIZATION IS ACHIEVED BY COUNTING BOTH CORRECT AND INCORRECT DECISIONS IN AN UP/DOWN COUNTER LOCATED AT U9 AND U10. THESE DECISIONS ARE SAMPLED EACH 16TH CLOCK TIME BY THE OUTPUT OF THE DIVIDE-BY-SIXTEEN COUNTER AT U18. THE PURPOSE OF COUNTING ONLY EVERY 16TH DECISION IS THAT IT MAKES THE CIRCUIT IMMUNE TO A BURST OF ERRORS, YET PROVIDES A VERY FAST MEANS OF DETERMINING WHETHER THE CIRCUIT IS IN OR OUT OF SYNCHRONIZATION. EACH CORRECT DECISION RESULTS IN A COUNT OF ONE IN THE UP DIRECTION AND EACH INCORRECT DECISION RESULTS IN A DOWN COUNT OF TWO. THE TIMES TWO MULTIPLYING CIRCUIT IS LOCATED AT U17. ONCE THE COUNTER HAS REACHED A STATE OF 10 THE CONDITION OF IN-SYNC IS ESTABLISHED. FURTHER CORRECT DECISIONS WILL RESULT IN THE COUNTER CONTINUING IN THE UPWARD DIRECTION UNTIL THE STATE OF 20 IS REACHED. AT THAT TIME THE SIGNAL UP INHIBIT (U2-11) IS ESTABLISHED AND FURTHER INCREMENTING OF THE COUNTER IS INHIBITED. THE INCORRECT DECISIONS RESULT IN DECREMENTING OF THE COUNTER AND WHEN THE COUNT OF TEN OR LESS IS REACHED, THE CONDITION OF OUT-OF-SYNC IS ESTABLISHED. EACH FURTHER INCORRECT DECISION RESULTS IN A DOWN COUNT OF TWO. WHEN THE DECODE OF ZERO IS REACHED, THE DOWN INHIBIT SIGNAL IS ESTABLISHED AT U3-8 AND FURTHER DECREMENTING IS INHIBITED.

When the out-of-sync exists, a resync request is generated at U19-13. This signal consists of the signals generated at U27 and the enabling signal at U11-5. This resync request signal is used to enable the feedforward data into the shift register. The feedforward data are received data (demux data) located at U26-9. The data are fed forward for a period of time exceeding 20 bits. This time period is established by the one-shot at U28. The process of feeding forward will continue to occur until the in-sync condition has been established.

PR Sync - Input/Output Signal Designations

PN Clock --- This clock is received from the Demux PC board and has an average frequency of 1.544 MHz.

Demux Data --- This is the demultiplexed data received from the Demux PC board. These data have an average bit rate of 1.544 MHz.

Bit Error--- This is an RZ output and is the signal that is sent to the error counters indicating that a bit error has occurred.

No Sync --- The signal is used to drive the No Sync LED indicator on the front panel and indicates that the internal generator pattern and the incoming data are out of synchronization.

PR Sync --- This is an RZ pulse that occurs per pseudo-random frame and is available on the rear-panel output jack labeled PR Sync. The amplitude of this pulse is approxi-

MATELY 2.5 VOLTS INTO A 75 OHM LOAD. THE WIDTH OF THE PULSE IS APPROXIMATELY 324 NS. THE RATE AT WHICH THE PULSE OCCURS, AS MEASURED ON AN AVERAGING FREQUENCY METER, IS 1.47 HZ.

TEST POINT 1 --- THIS IS THE RESYNC REQUEST LINE AND IS NORMALLY A LOGICAL 0 WHEN NOT REQUESTING.

TEST POINT 2 --- THIS IS THE DATA MODIFIER FOR THE FOURTEEN ZERO CONSTRAINT LIMIT. THIS SIGNAL OCCURS 31 TIMES DURING THE PSEUDORANDOM SEQUENCE.

TEST POINT 3-BIT ERROR --- THIS IS THE RZ OUTPUT WHICH RESULTS EACH TIME A NON-COMPARISON OCCURS.

TEST POINT 4 --- THIS IS THE RESYNC REQUEST OSCILLATOR. THIS SIGNAL HAS A FREQUENCY OF 4.3 KHZ AND A DUTY CYCLE OF 67%. THIS SIGNAL IS GATED THROUGH U19 BY THE OUT-OF-SYNC SIGNAL AT U11-6. THE FREQUENCY OF THIS OSCILLATOR IS CHOSEN IN SUCH A WAY THAT IT PROVIDES ENOUGH TIME TO ALLOW AT LEAST 20 BITS OF INFORMATION TO BE FED FORWARD AND TO PERFORM ENOUGH COMPARISONS TO DETERMINE IF AN IN-SYNC OR OUT-OF-SYNC CONDITION STILL EXISTS.

TEST POINT 5 --- THIS SIGNAL ESTABLISHES THE AMOUNT OF TIME THAT THE FEED FORWARD DATA ARE ENABLED.

ERROR ACCUMULATOR THEORY OF OPERATION

ERROR-RATE COUNTER -- THE ERROR-RATE MEASUREMENT IS MADE OVER A MANUALLY SELECTED TIME-BASE PERIOD. THE 3 DIGIT ERROR (U24 AND U29) COUNTS THE ERRORS OVER THIS SELECTED TIME BASE. AT

THE END OF THE TIME BASE THE SIGNAL SAMPLE IS GENERATED. AT THE END OF THE SAMPLE PULSE, THE SIGNAL RESET-1 IS GENERATED (U9-2) TO CLEAR THE COUNTER. THE SIGNAL DISPLAY BER ENABLES THE REGISTERS (U28 AND U25) TO OUTPUT THEIR CONTENTS TO THE DATA BUS. THIS ERROR RATE INFORMATION IS STROBED INTO THE DISPLAY ONCE EACH SECOND FOR SELECTED TIME BASES OF 10^{-4}, 10^{-5} AND 10^{-6} AND AT THE END OF THE TIME BASE FOR SELECTIONS OF 10^{-7} AND 10^{-8}.

TIME BASE COUNTER-- THE TIME BASE COUNTER ESTABLISHES THE PERIOD OF TIME OVER WHICH AN ERROR RATE MEASUREMENT IS MADE. BIT PERIODS OF TIME RANGING FROM 10^4 THROUGH 10^8 ARE MANUALLY SELECTED VIA U22 AND U23. THE TIME BASE COUNTER CONSISTS OF AN 8-STAGE DECADE COUNTER AT U16, U17, U14, AND U15 WITH SELECTABLE OUTPUT TAPS. AT THE END OF A SELECTED TIME BASE PERIOD, TWO CONTROL PULSES (SAMPLE AND RESET-1) ARE FORMED BY THE ONE-SHOT AT U1. THESE PULSES ARE USED TO STROBE THE CONTENTS OF THE ERROR COUNTER INTO A HOLDING REGISTER AND RESET THE COUNTER FOR THE NEXT MEASUREMENT PERIOD, RESPECTIVELY.

TOTAL ERROR COUNTER -- A TOTALIZING ERROR COUNTER, CONSISTING OF 5 STAGES, IS LOCATED AT U12 AND U32. THIS COUNTER ACCUMULATES ERRORS AS LONG AS THE SIGNAL COUNT ENABLE IS VALID (LOGIC "0") AT U31-1. THE TYPE OF ERROR BEING COUNTED (BIT/BIPOLAR) IS SELECTED BY GATES (U31 AND U30) AND APPLIED TO U21-13. IF THE TOTALIZED ERRORS ARE TO BE DISPLAYED, THEY ARE TRANSFERRED FROM THE COUNTER TO THE DATA BUS VIA THE GATES AT U20, U36, AND U33. THE SIGNAL CONTROLLING THIS TRANSFER IS DISPLAY TOTAL.

ERROR-SECOND COUNTER --- A TOTALIZING ERROR-SECOND COUNTER, CONSISTING OF 5 STAGES IS LOCATED AT U12, U27, AND U26. THIS

COUNTER COUNTS ONE-SECOND WIDE PULSES THAT ARE INITIATED BY THE RECEIVED ERRORS. THE TYPE OF ERROR-SECONDS BEING COUNTED IS DETERMINED BY THE SELECTED ERROR MODE (BIT/BIPOLAR). IF THE ERROR-SECONDS ARE TO BE DISPLAYED, THEY ARE TRANSFERRED FROM THE COUNTER TO THE DATA BUS VIA THE GATES AT U20,U35, AND U34. THE SIGNAL CONTROLLING THIS TRANSFER IS DISPLAY ES.

ERROR-SECOND TIMER -- THE ONE SECOND PULSE REQUIRED BY THE ERROR-SECOND COUNTER IS FORMED BY ENABLING (UPON RECEIPT OF AN ERROR) A DIVIDE BY THE 2^{14} COUNTER (U2 AND U5) WHICH HAS AS ITS CLOCK A CRYSTALL CONTROLLED 32,768 Hz TIMER OSCILLATOR LOCATED ON THE TIMER PCB. THE COUNTER IS ENABLED UNTIL A COUNT OF 32,768 IS REACHED (WHICH OCCURS AFTER 1 SEC OF TIME). AT THE END OF THIS COUNT, THE CIRCUIT IS RESET AND IS READY TO BE INITIATED AGAIN BY THE NEXT OCCURRENCE OF AN ERROR.

ERROR ACCUMULATOR INPUT/OUTPUT SIGNAL DESIGNATIONS

D1 THROUGH D80,000---DCD --- BCD WEIGHTED DATA THAT REPRESENT THE ERROR COUNT.

BIT ERROR OUT---REAR-PANEL OUTPUT WITH A NOMINAL LEVEL OF 2.5V INTO 75 OHMS. OUTPUT IS AN RZ PULSE WITH A WIDTH OF APPROXIMATELY 324 NS AND OCCURS EACH TIME A BIT ERROR IS RECEIVED.

COUNT---REAR-PANEL OUTPUT WITH A NOMINAL LEVEL OF 2.5 VOLTS INTO 75 OHMS. OUTPUT IS AN RZ PULSE WITH A WIDTH APPROXIMATELY 324 NS AND OCCURS EACH TIME THE ERROR COUNTER IS INCREMENTED.

COUNT ENABLE --- INPUT SIGNAL FROM THE TIMER PCB, WHICH, WHEN AT A LOGIC HIGH LEVEL, ENABLES THE SELECTED TYPE OF ERRORS TO BE COUNTED.

ERROR-SEC (L)--- FRONT-PANEL SWITCH SELECTION, WHICH, WHEN AT A LOGIC LOW LEVEL, ENABLES THE ERROR-SECOND MEASUREMENT FUNCTIONS.

BIT ERROR--- RZ INPUT PULSES WHICH ARE GATED, AS BIT ERRORS, TO THE ERROR COUNTER BY THE COMPLEMENT OF THE BPV ENABLE CONTROL SIGNAL.

BPV ENABLE--- FRONT-PANEL SWITCH SELECTION. A LOGIC LOW LEVEL SELECTS BIPOLAR VIOLATIONS TO BE COUNTED AND A LOGIC HIGH LEVEL SELECTS BIT ERRORS TO BE COUNTED.

BPV--- RZ INPUT PULSES WITH A WIDTH COMMENSURABLE WITH THE SELECTED INCOMING DS DATA. EACH PULSE REPRESENTS A DETECTED BIPOLAR VIOLATION.

DS CLOCK-1 --- CLOCK RECOVERED FROM THE RECEIVED BIPOLAR DATA. THE RATE OF THIS CLOCK IS THE SAME AS THE DS DATA RATE. THIS CLOCK IS USED WHEN MAKING BIPOLAR ERROR RATE MEASUREMENTS.

PN CLOCK ---CLOCK USED DURING THE DEMULTIPLEX PROCESS. THE AVERAGE RATE OF THIS CLOCK IS 1.544MHZ. THIS CLOCK IS USED WHEN MAKING BIT ERROR RATE MEASUREMENTS.

CLOCK--- REAR-PANEL OUTPUT WITH A NOMINAL LEVEL OF 2.5 VOLTS INTO 75 OHMS. THE CLOCK PRESENT AT THIS OUTPUT IS SELECTED VIA THE TYPE OF ERRORS BEING MEASURED (BIT/BIPOLAR) TO BE EITHER THE PN CLOCK OR THE DS CLOCK-1, RESPECTIVELY.

10^{-4} THROUGH 10^{-8}--- FRONT-PANEL SWITCH SELECTION THAT IS ACTIVE WHEN AT A LOGIC ZERO LEVEL. THESE INPUTS SELECT THE TIME BASE OVER WHICH A TIME RATE MEASUREMENT IS TO BE MADE.

TOTAL --- FRONT-PANEL SWITCH SELECTION THAT IS ACTIVE WHEN AT A LOGIC ZERO LEVEL. THIS SIGNAL SELECTS THE TOTALIZE FUNCTIONS.

MR--- POSITIVE PULSE INPUT THAT IS USED TO CLEAR THE ERROR COUNTER AND TIME BASE COUNTER.

STROBE (H) --- POSITIVE PULSE OUTPUT THAT IS USED BY THE TIMER PCB TO BLANK THE TEST IN PROCESS LED AT THE DISPLAY UPDATE TIME.

STROBE (L) --- ZERO GOING PULSE OUTPUT THAT IS USED TO UPDATE THE DISPLAY.

1 SEC--- PULSE INPUT WITH A PERIOD OF 1 SECOND. THIS SIGNAL IS USED TO INITIATE A DISPLAY UPDATE DURING TIME RATE MEASUREMENTS FOR A TIME BASE OF 10^4, 10^5, AND 10^6.

BLANK DIGIT 1,2,(H)--- OUTPUT SIGNAL USED TO BLANK DIGITS 1 AND 2 OF THE DISPLAY DURING TIME RATE MEASUREMENTS AND/OR ILLEGAL CHANNEL SELECTION.

BLANK DIGIT 3,4,5(L)--- OUTPUT SIGNAL USED TO BLANK DIGITS 3,4,5 OF THE DISPLAY AT A 1 SEC RATE DURING ILLEGAL CHANNEL SELECTION.

OSC --- 32.768 KHZ CLOCK INPUT SIGNAL THAT IS COUNTED DOWN TO FORM A PRECISE 1 SECOND PULSE WHICH IS USED DURING AN ERROR-SECOND MEASUREMENT.

Overflow --- Output bit that indicates an overflow associated with the front-panel display data.

Timer Theory of Operation

Time Interval --- The test time interval is timed by counting down from a preset value, (front-panel thumbwheel switch) using a two-stage minutes counter and a three-stage hours counter until each counter is at its minimum count (BCD 00 and 000, respectively). Until the hours counter is at a count of zero, it is decremented, by one count, each time the minutes counter reaches a state of zero. In addition to decrementing the hours count, the minutes counter is preset to a state of 60. The one minute time interval is clock (TP-3) derived from a crystal controlled 1 Hz clock source (TP-2). This clock is generated with a recirculating type counter which is formed with a 60 bit shift register. The data input to the shift register is the Q output of the 60th state which has a normal logic 1 level. The 1 Hz clock causes the logical one data to be shifted into the last stage after 60 clock pulses (1 minute of time). The Q output changes state (1 to 0) and is fed through U11-3 as a reset to the shift register. Resetting of the shift register will cause the 60th stage Q to return to a logical 1. The minutes clock is taken from the 60th stage Q output and the width of the clock, which is a function of the propagation delay of U17 and U11, is typically 600 ns. The hours clock pulse (U11-11) is generated each time the two stage minutes counter reaches its minimum count.

The basic 1 Hz clock signal is generated from a 32.768 kHz crystal controlled oscillator which is counted down by a

16-STAGE BINARY COUNTER. THE OSCILLATOR (LESS EXTERNAL FREQUENCY COMPONENTS) AND COUNTER ARE CONTAINED IN A SINGLE IC LOCATED AT U21. THE CRYSTAL OPERATES IN THE PARALLEL MODE, IN A CIRCUIT COMMONLY CALLED A PIERCE OSCILLATOR. THIS TYPE OF OSCILLATOR CONSISTS OF A SINGLE INVERTER CONNECTED TO GIVE THE NECESSARY 180^{0} FEEDBACK REQUIRED FOR OSCILLATION. THE CRYSTAL, WHOSE DRIVE IS CONTROLLED BY R_3, IS CONNECTED BETWEEN THE INVERTER OUTPUT AND INPUT, WITH TWO PHASE SHIFT CAPACITORS C_2 AND C_3.

TWO ON-BOARD MEANS HAVE BEEN PROVIDED TO AID IN TESTING THE TIMER CIRCUIT. SWITCH S1 LABELED NORM/TEST PROVIDES EITHER 1 Hz (NORM) OR 16 Hz (TEST) CLOCK OUTPUT AT U21-5 (TP-2). THE MINUTES COUNT CAN BE CHANGED TO SECONDS, BY GROUNDING TP-5.

ERROR COUNT/TIME REMAINING --- A DUAL 20-BIT DATA MULTIPLEXER (U1 THROUGH U5) PROVIDES A MEANS OF DISPLAYING THE CURRENT VALUE CONTAINED IN THE TIME INTERVAL COUNTER. THIS FEATURE ALLOWS THE USER TO DISPLAY IN HOURS AND MINUTES THE TIME REMAINING IN A TIMED MEASUREMENT.

LOST POWER MONITOR --- A.C. VOLTAGE, PRODUCED BY THE POWER SUPPLY'S INPUT TRANSFORMER, IS CONNECTED THROUGH A CURRENT LIMITING RESISTOR TO THIS PCB. THIS A.C. SIGNAL IS USED TO DRIVE AN OPTICAL ISOLATOR (U8) WHOSE OUTPUT KEEPS THE RETRIGGERABLE ONE-SHOT U3 IN A TRIGGERED STATE. IF THE A.C. INPUT IS LOST OR THE TEST SET IS BEING TURNED ON INITIALLY, THE Q OUTPUT OF U3 WILL MAKE A TRANSITION FROM A LOGICAL 0 TO A LOGICAL 1. THIS EVENT IS RECORDED ON THE FRONT-PANEL DISPLAY PCB AS A LOST POWER CONDITION. IF THE +5 VOLTS HAS DEGRADED TO AN UNUSEABLE LEVEL THE TRANSITION IS DELAYED BY R119/C38, UNTIL THE +5 VOLT SUPPLY HAS HAD A CHANCE TO STABILIZE.

Timer - Input/Output signal designations

Strobe Display --- Input pulse which initiates the blanking of the test in process LED for 120 ms each time the display is updated during error rate measurements.

Time to Go --- Front-panel switch control used to select which of the two 20-bit word inputs (error count/time) will be gated through the data selector to the front-panel display.

D1 through D8000 --- BCD weighted data input from the error counter.

C1 through C80000 --- BCD weighted data output. The contents of these data (error count/time) are controlled by the Time-To Go input described above.

M1 through M80 --- BCD weighted input that represents the number of minutes over which a timed measurement will be made. Value controlled via front-panel thumbwheel switches.

H1 through H800 --- Same as above (M1 through M80) except is hours input.

OSC --- Buffered 32.768 kHz clock output used by Error counter PCB during an error-sec measurement.

Untimed --- Front-panel switch control (active ground level) that is valid when either TOTAL or ERROR-SEC measurements are selected.

START/RESET --- FRONT-PANEL SWITCH CONTROL THAT INITIATES A TIMED MEASUREMENT IF THE TIMED FUNCTION HAS BEEN SELECTED. THIS INPUT WILL GENERATE A MASTER RESET PULSE TO THE ERROR COUNTER DURING ALL MODES OF OPERATION.

MR--- MASTER RESET (SEE ABOVE) PULSE. USED BY ERROR COUNTER.

1 SEC.--- 1 HZ OUTPUT SIGNAL USED TO UPDATE THE ERROR COUNT BEING DISPLAYED ON THE FRONT PANEL.

TEST IN PROCESS--- OUTPUT DRIVE SIGNAL FOR TEST IN PROCESS LED.

A.C. --- CURRENT LIMITED A.C. INPUT. INPUT FOR LOSS OF AC POWER MONITOR.

LOST POWER --- OUTPUT SIGNAL THAT IS A TRANSITION FROM A LOW TO HIGH LEVEL. INDICATES THAT THE AC INPUT VOLTAGE WAS ABSENT FOR A PERIOD OF TIME WHICH EXCEEDED ALLOWED AMOUNT.

DISPLAY THEORY OF OPERATION

THE FIVE-DIGIT DISPLAY IS FORMED BY INDIVIDUAL NUMERIC DISPLAYS WHICH CONTAIN THE NECESSARY LOGIC AND DRIVERS TO CONVERT AND DISPLAY THE BCD INPUT INFORMATION. DURING TIME RATE MEASUREMENTS ONLY THE RIGHT THREE DIGITS ARE USED TO DISPLAY THE ERROR COUNT. THE OTHER TWO DIGITS ARE BLANKED DURING THIS MODE BY THE SIGNAL BLANK DIGIT 1,2,(H). TOTAL AND ERROR-SEC MEASUREMENTS UTILIZE ALL FIVE DIGITS OF THE DISPLAY. OVERFLOW OCCURS AFTER 999 OR 9999 FOR TIME RATE AND TOTAL/ERROR-SEC MEASUREMENTS, RESPECTIVELY. THE TIME REMAINING DURING A TIMED

MEASUREMENT IS DISPLAYED AS FIVE DIGITS OF HOURS AND MINUTES USING THE FORMAT HHH..MM.

THE STATUS OF CURRENT CONDITIONS IS DISPLAYED ON 6 LEDS WHICH ARE DRIVEN BY LOGIC CONTAINED ON OTHER PCB'S. EACH INDICATOR INPUT IS LOGIC OR'D BY A DIODE WITH THE LAMP TEST PUSH-BUTTON. THE TEST FUNCTION WILL FORCE ALL INDICATORS ON WITH-OUT INTERFERRING WITH THE NORMAL OPERATION OF THE TEST SET. FOUR OF THE STATUS FUNCTIONS ARE LATCHED BY THE FLIP-FLOP AT U7 AND U8. THESE FUNCTIONS ARE REFERRED TO AS HISTORY STATUS. THE LAMP TEST FUNCTION IS ALSO DIODE OR'D WITH THESE SIGNALS BUT THE STORAGE FLIP-FLOPS ARE CLEARED.

DISPLAY INPUT/OUTPUT SIGNAL DESIGNATIONS

C80000 THROUGH C1 --- BCD WEIGHTED DATA INPUT.

SELECT TIME TO GO--- INPUT SIGNAL THAT IS ACTIVE WHEN LOW. THIS SIGNAL WILL TURN ON THE DECIMAL POINTS WITHIN U3 AND U4.

STROBE --- WHEN LOW, THE DISPLAYED DATA FOLLOW THE DATA ON THE INPUT OF THE DISPLAY. WHEN HIGH, THE DATA DISPLAYED ARE HELD CONSTANT AND ARE UNAFFECTED BY NEW DATA AT THE INPUT.

BLANK DIGIT 3,4,5 --- WHEN LOW, BLANKS THE THREE RIGHT-HAND DIGITS.

BLANK DIGIT 1,2 --- WHEN LOW, BLANKS THE TWO LEFT-HAND DIGITS.

TEST IN PROCESS --- INPUT INDICATING THAT THE TEST SET IS MAKING A MEASUREMENT.

ALL ONES --- INPUT INDICATING THAT THE SELECTED DATA CHANNELS CONTAIN AN EXCESSIVE NUMBER OF CONSECUTIVE ONES.

X-BIT --- INPUT INDICATING THAT THE DS1C/DS2 ALARM DIGIT WAS FOUND TO BE IN A LOGIC ZERO STATE.

OUT OF FRAME--- INPUT INDICATING THAT THE TEST SET IS CURRENTLY OUT OF DS FRAME.

LOST FRAME --- INPUT TO LATCHING CIRCUIT INDICATES THAT THE TEST SET HAS BEEN OUT OF DS FRAME.

EXCESS ZEROS --- INPUT INDICATING THAT THE TEST SET IS CURRENTLY RECEIVING AN EXCESSIVE NUMBER OF CONSECUTIVE ZEROS IN THE INCOMING DS DATA.

LOST DATA --- INPUT TO LATCHING CIRCUIT WHICH INDICATES THAT AN EXCESSIVE NUMBER OF ZEROS HAVE BEEN DETECTED IN THE RECEIVER'S INPUT DATA.

NO SYNC --- INPUT INDICATING THAT THE RECEIVER'S INTERNAL PATTERN GENERATOR IS NOT SYNCHRONIZED WITH THE DEMULTIPLEXED CHANNEL DATA.

LOST SYNC --- INPUT TO LATCHING CIRCUIT WHICH INDICATES THAT THE RECEIVER HAS LOST DATA SYNCHRONIZATION.

SECTION 5
MAINTENANCE

GENERAL

This section contains the preventative and corrective maintenance procedures for the S5102 Error Rate Test Set Receiver.

Maintenance support data in the form of diagrams, tables, and descriptive material are provided in the other sections of this manual. A discussion of circuit theory is presented in Section 4. The latter part of this section contains individual parts lists for each of the seven circuit boards and the chassis (Tables 5-2 through 5-12). The functional block diagram, schematic diagrams, component locations, and internal wiring diagrams are located in Section 6. Refer to Appendix A for DC power supply information.

The user should be thoroughly familiar with the Test Set capabilities, theory of operation, and operating procedures before attempting any maintenance or troubleshooting procedures. Table 5-1 lists the required maintenance test equipment.

COMPONENT LOCATION

The physical location of the major components in the Test Set chassis is shown in Fig. 1-1. Figures 6-2, 6-3, 6-4, 6-5,

TABLE 5-1
TEST EQUIPMENT REQUIRED FOR MAINTENANCE
(BUT NOT SUPPLIED)

ITEM	TYPE	PURPOSE
OSCILLOSCOPE	TEKTRONIX MODEL 475 OR EQUIVALENT	MONITORING WAVEFORMS, SIGNAL LEVEL, ETC.
DIGITAL VOLTMETER	SIMPSON MODEL 461 OR EQUIVALENT DIGITAL MULTIMETER.	PRECISION VOLTAGE READINGS DURING ALIGNMENT PROCEDURES.
ELECTRONIC COUNTER	HP-5383A OR EQUIVALENT	FREQUENCY OR PERIOD MEASUREMENTS.

6-6, 6-7 AND 6-8 SHOW THE VARIOUS COMPONENTS ON CIRCUIT BOARDS A1, A2, A3, A4, A5, A6, AND A7, RESPECTIVELY.

PREVENTATIVE MAINTENANCE

PREVENTATIVE MAINTENANCE INCLUDES THE PERFORMANCE OF CHECKS AND SERVICE PROCEDURES WHICH PREVENT OR MINIMIZE DOWNTIME OF THE EQUIPMENT. THROUGH UTILIZATION OF SOLID STATE CIRCUITRY, THE CHECKS AND SERVICES ARE SIMPLIFIED, AND MAY BE LIMITED TO VISUAL INSPECTION FOR DEFECTIVE COMPONENTS, LOOSE HARDWARE AND/OR ACCUMULATION OF DUST WITHIN A UNIT AT CRITICAL AREAS.

MINOR REPAIR PROCEDURES

MINOR REPAIR PROCEDURES FOR THE TEST SET ARE LIMITED TO ITEMS

SUCH AS INDICATOR AND FUSE REPLACEMENT. THE NUMBER DISPLAYS AND INDICATORS MAY BE REPLACED BY UNFASTENING THE FRONT-PANEL CIRCUIT BOARD, REMOVING THE DEFECTIVE UNIT, AND INSERTING THE NEW LED OR DISPLAY. THE PANEL FUSE (3/4 AMPERE, SLO-BLO, 3AG), IS REPLACED AT THE UNIT FRONT PANEL BY REMOVING THE POWER CABLE AND SLIDING THE PLASTIC DOOR TO THE LEFT, PULLING THE TAB FORWARD AND EJECTING THE FUSE. PUSH THE REPLACEMENT FUSE INTO THE HOLDER, SLIDE THE DOOR TO THE RIGHT AND REPLACE THE POWER CABLE.

NOTE

IF A NEW FUSE BLOWS IMMEDIATELY AFTER REPLACEMENT, DETERMINE THE CAUSE OF THE PROBLEM BEFORE INSERTING ANOTHER FUSE.

CORRECTIVE MAINTENANCE

CORRECTIVE MAINTENANCE OF THE TEST SET CONSISTS OF REPAIRS OR ADJUSTMENTS THAT MUST BE MADE AFTER A MALFUNCTION OR FAILURE OCCURS TO RESTORE THE UNIT TO NORMAL OPERATION. THE CORRECTIVE MAINTENANCE REPAIRS SHOULD ONLY BE ATTEMPTED BY QUALIFIED PERSONNEL, KNOWLEDGEABLE IN SOLID-STATE LOGIC AND CIRCUIT THEORY AND, IN PARTICULAR, THOROUGHLY FAMILIAR WITH THE TEST SET THEORY OF OPERATION. NECESSITY FOR CORRECTIVE MAINTENANCE IS INDICATED WHEN ANY VARIATION FROM THE SPECIFIED OPERATIONS CRITERIA OF THE UNIT ARE NOTED. REFER TO TABLE 1-3 FOR A LIST OF REQUIRED TEST EQUIPMENT.

ADJUSTMENT PROCEDURES

THE ONLY TEST SET ADJUSTMENTS THAT MAY BE REQUIRED ARE THE DC POWER SUPPLY OUTPUT VOLTAGE AND THE FREQUENCY ADJUSTMENTS FOR THE INTERNAL OSCILLATORS. THE TEST SET CAN BE REMOVED FROM

ITS ENCLOSURE BY UNSCREWING THE FOUR KNURLED KNOBS ON THE FRONT PANEL AND THE TWO AT THE REAR (BOTTOM) OF THE ENCLOSURE. THE TEST SET CAN THEN BE SLID FROM ITS ENCLOSURE.

A. POWER SUPPLY ADJUSTMENT - REFER TO APPENDIX A FOR THE POWER SUPPLY ADJUSTMENT ON THE PS1 POWER SUPPLY.

B. OSCILLATOR FREQUENCY ADJUSTMENTS - (TO BE SUPPLIED BY ENGINEERING).

TROUBLESHOOTING PROCEDURES

TROUBLESHOOTING PROCEDURES SHOULD BE PERFORMED IN A LOGICAL SEQUENCE TO ISOLATE A MALFUNCTION TO A SPECIFIC LOCATION. FAMILIARIZATION WITH THE UNIT WILL ENABLE THE TECHNICAL PERSONNEL TO RAPIDLY ISOLATE THE PROBLEM AREA. THIS MAY BE ATTAINED WITH THE AID OF THE FUNCTIONAL CHARACTERISTICS, CIRCUIT THEORY DISCUSSIONS, SCHEMATIC AND COMPONENT DISCUSSIONS, AND SCHEMATIC AND COMPONENT DIAGRAMS PRESENTED IN SECTION 6 OF THIS MANUAL.

MALFUNCTIONS CAN BE GENERALLY LIMITED TO PRINTED CIRCUIT BOARDS PC1 AND PC3 THROUGH PC8 (REFER TO FIG. 1-1). ONCE ISOLATED TO A BOARD, INDIVIDUAL PLUG-IN COMPONENTS CAN BE MONITORED FOR CORRECT WAVEFORMS BY USING AN EXTENDER BOARD.

CAUTION

DO NOT MEASURE THE RESISTANCE OF SOLID STATE DEVICES. THE DEVICES MAY BE DAMAGED BY THE APPLICATION OF VOLTAGES WITH IMPROPER POLARITIES, OR BY THE HIGH SHORT-CIRCUIT CURRENT OF MOST VOLTOHMMETERS.

IF NORMAL OPERATION OF THE UNIT INDICATES A MALFUNCTION, THE FOLLOWING GENERAL ITEMS SHOULD BE CHECKED BEFORE BEGINNING A TROUBLESHOOTING PROCEDURE:

A. POWER IS APPLIED TO THE UNIT (RED POWER INDICATOR ILLUMINATES).

B. ALL INTERNAL AND EXTERNAL CONNECTORS ARE SECURELY MATED WITH PROPER RECEPTACLES.

C. ALL REQUIRED OUTPUT SIGNALS ARE BEING TRANSMITTED FROM THE TEST SET.

D. ALL FRONT-PANEL SWITCHES ARE PROPERLY SET FOR THE PARTICULAR FUNCTION TO BE PERFORMED.

TABLE 5-2

PARTS LIST FOR
INPUT AMPLIFIER/CLOCK RECOVERY
PRINTED CIRCUIT BOARD (PC6)

COMPONENT ITEM NO.	DESCRIPTION TRUNCATED
0022-2150	RES COMP 15 OHM 5P 1/4
0022-2430	RES COMP 43 OHM 5P 1/4
0022-2560	RES COMP 56 OHM 5P 1/4
0022-2750	RES COMP 75 OHM 5P 1/4
0022-2910	RES COMP 91 OHM 5P 1/4
0022-3100	RES COMP 100 OHM 5P 1/4
0022-3130	RES COMP 130 OHM 5P 1/4
0022-3200	RES COMP 200 OHM 5P 1/4
0022-3220	RES COMP 220 OHM 5P 1/4
0022-3270	RES COMP 270 OHM 5P 1/4
0022-3300	RES COMP 300 OHM 5P 1/4
0022-3330	RES COMP 330 OHM 5P 1/4
0022-3430	RES COMP 430 OHM 5P 1/4
0022-3510	RES COMP 510 OHM 5P 1/4
0022-3620	RES COMP 620 OHM 5P 1/4
0022-3680	RES COMP 680 OHM 5P 1/4
0022-3750	RES COMP 750 OHM 5P 1/4
0022-4100	RES COMP 1 KOHM 5P 1/4
0022-4180	RES COMP 1.8 KOHM 5P 1/4
0022-4300	RES COMP 3 KOHM 5P 1/4
0022-4390	RES COMP 3.9 KOHM 5P 1/4
0022-4430	RES COMP 4.3 KOHM 5P 1/4
0022-4510	RES COMP 5.1 KOHM 5P 1/4

COMPONENT ITEM NO.	DESCRIPTION TRUNCATED
0022-4820	RES COMP 8.2 KOHM 5P 1/4
0022-4910	RES COMP 9.1 KOHM 5P 1/4
0022-5100	RES COMP 10 KOHM 5P 1/4
0022-5110	RES COMP 11 KOHM 5P 1/4
0022-5130	RES COMP 13 KOHM 5P 1/4
0022-5200	RES COMP 20 KOHM 5P 1/4
0022-5270	RES COMP 27 KOHM 5P 1/4
0022-5300	RES COMP 30 KOHM 5P 1/4
0022-5330	RES COMP 33 KOHM 5P 1/4
0022-5510	RES COMP 51 KOHM 5P 1/4
0022-5750	RES COMP 75 KOHM 5P 1/4
0022-6160	RES COMP 160 KOHM 5P 1/4
0022-7100	RES COMP 1 MOHM 5P 1/4
0032-3100	RES COMP 100 OHM 5P 1/2
0110-2673	RES MFLM 67.3 OHM 1P 1/8
0110-3274	RES MFLM 274 OHM 1P 1/8W
0110-4110	RES MFLM 1.10 KOHM 1P 1/
0333-3500J	RES VAR 500 OHM 10P 1/2W
0333-5100C	RES VAR 10 KOHM 10P 1/2W
1013-6622	CAP CER 0.22 MFD 10P 50V
1013-6710	CAP CER 1.0 MFD 10P 50V
1013-8315	CAP CER 150 PF 10P 200V
1013-8510	CAP CER .01 MFD 20P 200V
1014-4610	CAP CER 0.1 MFD 20P 200V
1014-8410	CAP CER 1000 PF 20P 200V

COMPONENT ITEM NO.	DESCRIPTION TRUNCATED
1041-7311	CAP MICA 110 PF 2P 100V
1041-7322	CAP MICA 220 PF 2P 100V
1041-8233	CAP MICA 33 PF 2P 100V
1042-9250	CAP MICA 50 PF 5P 500V
1042-9313	CAP MICA 130 PF 5P 500V
1059-8253	CAP VAR 9-35 PF PCB MNT
1059-8260	CAP VAR 15-60 PF PC MNT
1064-1233	CAP MIN-TANT 33 MFD 10WV
1064-4210	CAP MIN-TANT 10 MFD 25WV
2112-4148	DIODE GEN PURPOSE IN4148
2161-0821	DIODE ZENER 6.2V 10P IN8
3221-2218	TRNSTR NPN AMPLIFIER 2N2
3224-3563A	TRNSTR NPN AMPLIFIER MPS
3224-4403	TRNSTR NPN AMPLIFIER 2N4
3224-5771	TRNSTR PNP RF AMPLIFIER
4012-10116	IC ECL MC10116P PLSTC
4012-74H52	IC TTL SN74H52N PLSTC
4012-74LS00	IC TTL SN74LS00N PLSTC
4012-74LS02	IC TTL SN74LS02N PLSTC
4012-74LS04	IC TTL SN74LS04N PLSTC
4012-74LS112	IC TTL SN74LS112N PLSTC
4012-74LS161	IC TTL SN74LS161N PLSTC
4012-74LS174	IC TTL SN74LS174N PLSTC
4012-74S133	IC TTL SN74S133N PLSTC

COMPONENT ITEM NO.	DESCRIPTION TRUNCATED
4012-7404	IC TTL SN7404N PLSTC
4012-7406	IC TTL SN7406N PLSTC
4012-74123	IC TTL SN74123N PLSTC
4012-74125	IC TTL SN74125N PLSTC
4012-7430	IC TTL SN7430N PLSTC
4100-1590	IC DIFF I/O VIDEO AMP MC
4160-0564	IC PLL 50 MHZ MAX NE564-
4163-72747	IC LINEAR OPAMP DUAL UA7
4311-5000	IC QUAD TRNSTR ARRAY SO5
5033-2215	INDCTR MLD 15 UH 10P
5043-2182	INDCTR MLD 8.2 UH 10P
5924-0256	XFMR DC ISOL TMOT2.5-6
7000-0004	RELAY 8 PIN DIP EI&S MS2
8000-9003	PIN PCB CONCORD 10-916-2
9111-0002	COMPONENT SPACER 8 LEAD
9601-0663	SS102RX INPUT AMP/CLK RE
9731-7243	RF SHIELD

TABLE 5-3

PARTS LIST FOR
FRAME SYNC PRINTED CIRCUIT BOARD (PC5)

COMPONENT ITEM NO.	DESCRIPTION TRUNCATED
0022-3200	RES COMP 200 OHM 5P 1/4
0022-4100	RES COMP 1 KOHM 5P 1/4
0022-4300	RES COMP 3 KOHM 5P 1/4
0022-4750	RES COMP 7.5 KOHM 5P 1/4
0022-4910	RES COMP 9.1 KOHM 5P 1/4
0022-5100	RES COMP 10 KOHM 5P 1/4
1013-8247	CAP CER 47 PF 10P 200V
1013-8315	CAP CER 150 PF 10P 200V
1013-8510	CAP CER .01 MFD 20P 200V
1064-1233	CAP MIN-TANT 33 MFD 10WV
2112-4148	DIODE GEN PURPOSE IN4148
3224-4403	TRNSTR NPN AMPLIFIER 2N4
4012-4000	IC CMOS MC14000BCP PLSTC
4012-4001	IC CMOS MC14001BCP PLSTC
4012-4011	IC CMOS MC14011BCP PLSTC
4012-4027	IC CMOS MC14027BCP PLSTC
4012-4028	IC CMOS MC14028BCP PLSTC
4012-4512	IC CMOS MC14512BCP PLSTC
4012-74LS00	IC TTL SN74LS00N PLSTC
4012-74LS02	IC TTL SN74LS02N PLSTC
4012-74LS04	IC TTL SN74LS04N PLSTC
4012-74LS08	IC TTL SN74LS08N PLSTC
4012-74LS10	IC TTL SN74LS10N PLSTC
4012-74LS112	IC TTL SN74LS112N PLSTC
4012-74LS123	IC TTL SN74LS123N PLSTC
4012-74LS155	IC TTL SN74LS155N PLSTC
4012-74LS160	IC TTL SN74LS160N PLSTC
4012-74LS162	IC TTL SN74LS162N PLSTC
4012-74LS175	IC TTL SN74LS175N PLSTC
4012-74LS20	IC TTL SN74LS20N PLSTC
4012-74LS27	IC TTL SN74LS27N PLSTC
4012-74LS54	IC TTL SN74LS54N PLSTC
4012-74LS74	IC TTL SN74LS74N PLSTC
4012-74LS86	IC TTL SN74LS86N PLSTC
4012-7402	IC TTL SN7402N PLSTC
4012-7405	IC TTL SN7405N PLSTC
9601-0527	S5102RX FRAME SYNC PCB

TABLE 5-4

PARTS LIST FOR
DEMULTIPLEXER PRINTED CIRCUIT BOARD (PC7)

COMPONENT ITEM NO.	DESCRIPTION TRUNCATED
0022-2120	RES COMP 12 OHM 5P 1/4
0022-2750	RES COMP 75 OHM 5P 1/4
0022-3100	RES COMP 100 OHM 5P 1/4
0022-4100	RES COMP 1 KOHM 5P 1/4
0022-4180	RES COMP 1.8 KOHM 5P 1/4
0022-5100	RES COMP 10 KOHM 5P 1/4
0822-5100	RES SIP 8PIN 10 KOHM 2P
1013-7382	CAP CER 820 PF 10P 50V
1013-8310E	CAP CER 100 PF 20P 100V
1013-8510	CAP CER .01 MFD 20P 200V
1064-1233	CAP MIN-TANT 33 MFD 10WV
1064-4210	CAP MIN-TANT 10 MFD 25WV
3224-5771	TRNSTR PNP RF AMPLIFIER
4012-74LS00	IC TTL SN74LS00N PLSTC
4012-74LS02	IC TTL SN74LS02N PLSTC
4012-74LS04	IC TTL SN74LS04N PLSTC
4012-74LS11	IC TTL SN74LS11N PLSTC
4012-74LS112	IC TTL SN74LS112N PLSTC
4012-74LS20	IC TTL SN74LS20N PLSTC
4012-74LS74	IC TTL SN74LS74N PLSTC
4012-74LS86	IC TTL SN74LS86N PLSTC
4012-7406	IC TTL SN7406N PLSTC
4012-7425	IC TTL SN7425N PLSTC
8000-9003	PIN PCB CONCORD 10-916-2
9601-0547	S5102RX DEMUX PCB

TABLE 5-5

PARTS LIST FOR
PR SYNC PRINTED CIRCUIT BOARD (PC4)

COMPONENT ITEM NO.	DESCRIPTION TRUNCATED
0022-2120	RES COMP 12 OHM 5P 1/4
0022-2750	RES COMP 75 OHM 5P 1/4
0022-3200	RES COMP 200 OHM 5P 1/4
0022-4100	RES COMP 1 KOHM 5P 1/4
0022-4180	RES COMP 1.8 KOHM 5P 1/4
0022-4300	RES COMP 3 KOHM 5P 1/4
0022-5100	RES COMP 10 KOHM 5P 1/4
0022-5120	RES COMP 12 KOHM 5P 1/4
0022-5150	RES COMP 15 KOHM 5P 1/4
1013-8322	CAP CER 220 PF 20P 200V
1013-8510	CAP CER .01 MFD 20P 200V
1014-8447	CAP CER 4700 PF 20P 100V
1064-1233	CAP MIN-TANT 33 MFD 10WV
1064-4210	CAP MIN-TANT 10 MFD 25WV
3224-4403	TRNSTR NPN AMPLIFIER 2N4
3224-5771	TRNSTR PNP RF AMPLIFIER
4012-74LS00	IC TTL SN74LS00N PLSTC
4012-74LS02	IC TTL SN74LS02N PLSTC
4012-74LS04	IC TTL SN74LS04N PLSTC
4012-74LS10	IC TTL SN74LS10N PLSTC
4012-74LS123	IC TTL SN74LS123N PLSTC
4012-74LS175	IC TTL SN74LS175N PLSTC
4012-74LS30	IC TTL SN74LS30N PLSTC
4012-74LS74	IC TTL SN74LS74N PLSTC
4012-74LS86	IC TTL SN74LS86N PLSTC
4012-7406	IC TTL SN7406N PLSTC
4012-7408	IC TTL SN7408N PLSTC
4012-74161	IC TTL SN74161N PLSTC
4012-74192	IC TTL SN74192N PLSTC
4012-7474	IC TTL SN7474N PLSTC
4160-0555	IC LINEAR NE555N
8000-9003	PIN PCB CONCORD 10-916-2
9601-0528	S5102RX PR SYNC PCB

TABLE 5-6

PARTS LIST FOR
ERROR ACCUMULATOR PRINTED CIRCUIT BOARD (PC3)

COMPONENT ITEM NO.	DESCRIPTION TRUNCATED
0012-3200	RES COMP 200 OHM 5P 1/8
0022-2120	RES COMP 12 OHM 5P 1/4
0022-2750	RES COMP 75 OHM 5P 1/4
0022-3270	RES COMP 270 OHM 5P 1/4
0022-4100	RES COMP 1 KOHM 5P 1/4
0022-4180	RES COMP 1.8 KOHM 5P 1/4
0022-5100	RES COMP 10 KOHM 5P 1/4
0821-4470	RES SIP 8PIN 4.7 KOHM 2P
0822-5100	RES SIP 8PIN 10 KOHM 2P
1013-8247	CAP CER 47 PF 10P 200V
1013-8333	CAP CER 330 PF 10P 200V
1013-8510	CAP CER .01 MFD 20P 200V
1064-1233	CAP MIN-TANT 33 MFD 10WV
1064-4210	CAP MIN-TANT 10 MFD 25WV
3224-5771	TRNSTR PNP RF AMPLIFIER
4012-4013	IC CMOS MC14013BCP PLSTC
4012-4020	IC CMOS MC14020BCP PLSTC
4012-4049	IC CMOS MC14049BCP PLSTC
4012-4538	IC CMOS MC14538BCP PLSTC
4012-74C244	IC CMOS MM74C244
4012-74C373	IC CMOS MM74C373
4012-74LS04	IC TTL SN74LS04N PLSTC
4012-7400	IC TTL SN7400N PLSTC
4012-7402	IC TTL SN7402N PLSTC
4012-7404	IC TTL SN7404N PLSTC
4012-7406	IC TTL SN7406N PLSTC
4012-7410	IC TTL SN7410N PLSTC
4012-74123	IC TTL SN74123N PLSTC
4012-74125	IC TTL SN74125N PLSTC
4012-74390	IC TTL SN74390N PLSTC
4012-7474	IC TTL SN7474N PLSTC
8000-9003	PIN PCB CONCORD 10-916-2
9601-0619	S5102RX ERROR ACCUMULATO

TABLE 5-7

PARTS LIST FOR
TIMER PRINTED CIRCUIT BOARD (PC8)

COMPONENT ITEM NO.	DESCRIPTION TRUNCATED
0022-3200	RES COMP 200 OHM 5P 1/4
0022-4100	RES COMP 1 KOHM 5P 1/4
0022-4150	RES COMP 1.5 KOHM 5P 1/4
0022-4300	RES COMP 3 KOHM 5P 1/4
0022-5100	RES COMP 10 KOHM 5P 1/4
0022-5150	RES COMP 15 KOHM 5P 1/4
0022-5390	RES COMP 39 KOHM 5P 1/4
0022-6470	RES COMP 470 KOHM 5P 1/4
0022-8220	RES COMP 22 MOHM 5P 1/4
0822-5100	RES SIP 8PIN 10 KOHM 2P
1013-8310	CAP CER 100 PF 20P 200V
1013-8510E	CAP CER .01 MFD 20P 100V
1014-4610	CAP CER 0.1 MFD 20P 200V
1042-9227	CAP MICA 27 PF 5P 100V
1059-8253	CAP VAR 9-35 PF PCB MNT
1064-1233	CAP MIN-TANT 33 MFD 10WV
1064-4210	CAP MIN-TANT 10 MFD 25WV
2112-4148	DIODE GEN PURPOSE IN4148
3224-4403	TRNSTR NPN AMPLIFIER 2N4
4012-4001	IC CMOS MC14001BCP PLSTC
4012-4011	IC CMOS MC14011BCP PLSTC
4012-4013	IC CMOS MC14013BCP PLSTC
4012-4023	IC CMOS MC14023BCP PLSTC
4012-4049	IC CMOS MC14049BCP PLSTC
4012-4451	IC CMOS MC14451BCP PLSTC
4012-4522	IC CMOS MC14522BCP PLSTC
4012-4538	IC CMOS MC14538BCP PLSTC
4012-4557	IC CMOS MC14557BCP PLSTC
4012-74123	IC TTL SN74123N PLSTC
4012-74157	IC TTL SN74157N PLSTC
4760-0111	IC OPTO-COUPLER TIL111
6000-6128	XTAL 32.768 KHZ
8000-9003	PIN PCB CONCORD 10-916-2
9201-0002	SWITCH SLIDE DPDT MSS225
9306-0009	CONN PCB HDR MALE RTAGL
9601-0589	S5102RX TIMER PCB

TABLE 5-8

PARTS LIST FOR FRONT PANEL

COMPONENT ITEM NO.	DESCRIPTION TRUNCATED
8000-0001	SCREW PNHD MET NO.2-56X1
8000-0005	SCREW PNHD MET NO.2-56X1
8000-0045	SCREW PNHD MET NO.4-40X3
8000-0083	SCREW PNHD MET NO.6-32X1
8000-0086	SCREW PNHD MET NO.6-32X7
8000-0147	SCREW PNHD MET NO.10-32X
8000-0404	WASHER FIBRE BLACK HHS 2
8000-1000	NUT HEX MET NO.2-56
8000-1200	LOCKWASHER NO.2
8000-1202	LOCKWASHER NO.4
8000-1204	LOCKWASHER NO.6
8000-1206	LOCKWASHER NO.10
8000-1509	LUG SOLDER ANGLE NO.10
9000-0002	LINE FILTER 6J4
9000-0002A	CORCOM 6J4 .125 PANEL CL
9000-0105	FUSE 3/4A SLO-BLO 3AG
9190-0002	HANDLE HHS 2052
9200-0014	SWITCH TOGGLE SPDT CK710
9203-0000	SWITCH PB MMNTRY SPST CK
9203-0100	SWITCH PB DPDT 2XFA17.5
9203-0101	SWITCH PB DPDT 4XFA17.5
9205-0009	SWITCH PB POWER ON/OFF
9310-0004	PATCH JACK TYPE 310
9541-7148	S5102RX DISPLAY BD PCB A
9541-7185	S5102RX PUSHBUTTON SW PC
9541-7188	S5102RX THUMBWHL SW PCB
9701-7134	S5102RX WECO F/P FINISHE
9701-7137	SWITCH BRACKET
9701-7192	S5102RX WECO NAMEPLATE
9701-7196	SWITCH BRACKET
9721-7135	DISPLAY WINDOW
9721-7136	310 MOUNTING BLOCK

TABLE 5-9

PARTS LIST FOR DISPLAY BOARD

COMPONENT ITEM NO.	DESCRIPTION TRUNCATED
0022-3270	RES COMP 270 OHM 5P 1/4
0022-4100	RES COMP 1 KOHM 5P 1/4
0022-5100	RES COMP 10 KOHM 5P 1/4
1013-8510	CAP CER .01 MFD 20P 200V
1064-1233	CAP MIN-TANT 33 MFD 10WV
2112-4148	DIODE GEN PURPOSE IN4148
2274-4555	DIODE LED YELLOW HP5082-
2274-4655	DIODE LED RED HP5082-465.
2274-4955	DIODE LED GREEN HP5082-4
4012-7405	IC TTL SN7405N PLSTC
4012-7408	IC TTL SN7408N PLSTC
4012-7474	IC TTL SN7474N PLSTC
4513-0308	IC DISPLAY TIL308
4513-0309	IC DISPLAY TIL309
9000-2905	SPACER NYLON 3/160D X 1/
9203-0005	SWITCH PB DPDT CK8221
9300-0030	SOCKET IC 16 PIN LOW PRO
9303-0003	CONN POST MALE
9306-0012	CONN PCB HDR 16 PIN 0.06
9305-0032	CONN PCB HDR MALE RTAGL
9601-0542	S5102RX DISPLAY PCB

TABLE 5-10

PARTS LIST FOR MOTHERBOARD

COMPONENT ITEM NO.	DESCRIPTION TRUNCATED
0022-3240	RES COMP 240 OHM 5P 1/4
0022-4100	RES COMP 1 KOHM 5P 1/4
0333-3500J	RES VAR 500 OHM 10P 1/2W
1014-4610	CAP CER 0.1 MFD 20P 200V
1064-4210	CAP MIN-TANT 10 MFD 25WV
4200-0317K	IC LINEAR REGULATOR LM31
8000-0045	SCREW PNHD MET NO.4-40X3
8000-1002	NUT HEX MET NO.4-40
8000-1202	LOCKWASHER NO.4
9300-0119	CONN EDGE DUAL 50 POS PC
9306-0013	CONN PCB HDR 16 PIN 0.12
9306-0027	CONN PCB HDR MALE STRT 2
9313-0001	CONN EDGE DUAL 22 POS PC
9601-0531	S5102RX MOTHER BD PCB

TABLE 5-11
PARTS LIST FOR
WIRING ASSEMBLY

COMPONENT ITEM NO.	DESCRIPTION TRUNCATED
0012-5330	RES COMP 33 KOHM 5P 1/8W
0110-3392	RES MFLM 392 OHM 1P 1/8W
0120-2332	RES MFLM 33.2 OHM 1P 1/4
8000-3200	CABLE CLAMP PLASTIC 1/8
8000-9008	CORCOM MOLEX PIN 0205120
9511-7151	S5102RX WECO FRONT PANEL
9531-7239	S5102RX CHASSIS ASSY: ME
9551-7164	CABLE ASSY FLAT 40 POS
9551-7175	CABLE ASSY FLAT 40 POS
9551-7177	CABLE ASSY FLAT 16 POS
9551-7178	CABLE ASSY FLAT 16 POS
9551-7244	S5102RX WECO AC/DC HARNE
9551-7258	CABLE ASSY COAXIAL
9551-7259	CABLE ASSY COAXIAL
9551-7260	CABLE ASSY COAXIAL
9551-7261	CABLE ASSY COAXIAL
9551-7262	CABLE ASSY COAXIAL
9551-7263	CABLE ASSY COAXIAL
9551-7264	CABLE ASSY COAXIAL

TABLE 5-12

PARTS LIST FOR CHASSIS

COMPONENT ITEM NO.	DESCRIPTION TRUNCATED
8000-0045	SCREW PNHD MET NO.4-40X3
8000-0084	SCREW PNHD MET NO.6-32X5
8000-0085	SCREW PNHD MET NO.6-32X3
8000-0116	SCREW PNHD MET NO.8-32X7
8000-0117	SCREW PNHD MET NO.8-32X1
8000-0122	SCREW PNHD MET NO.8-32X1
8000-1004	NUT HEX MET NO.6-32
8000-1005	NUT HEX MET NO.8-32
8000-1202	LOCKWASHER NO.4
8000-1204	LOCKWASHER NO.6
8000-1205	LOCKWASHER NO.8
8000-1302	FLAT WASHER MET NO.4
8000-1305	FLAT WASHER MET NO.8
8000-2312	SPACER MET HEX THD 4-40X
9070-0512	POWER SUPPLY H88512
9310-0004	PATCH JACK TYPE 310
9541-7117	S5102RX MOTHER BD PCB AS
9701-7222	S5102 SUPPORT BRACKET
9701-7237	S5102RX INNER CHASSIS MA
9721-7221	S5102 SUPPORT BLOCK

SECTION 6
DIAGRAMS

GENERAL

This section contains schematic diagrams and component location diagrams for the S5102 Error Rate Test Set (Receiver). Table 6-1 is an index of the illustrations that appear in this section.

TABLE 6-1
INDEX OF FIGURES

FIGURE

6-1 FUNCTIONAL BLOCK DIAGRAM

6-2 INPUT AMPLIFIER/CLOCK RECOVERY ASSEMBLY DRAWING AND SCHEMATIC.

6-3 FRAME SYNC ASSEMBLY DRAWING AND SCHEMATIC.

6-4 DEMUX ASSEMBLY DRAWING AND SCHEMATIC.

6-5 PR SYNC ASSEMBLY DRAWING AND SCHEMATIC.

6-6 ERROR ACCUMULATOR ASSEMBLY DRAWING AND SCHEMATIC.

6-7 TIMER ASSEMBLY DRAWING AND SCHEMATIC.

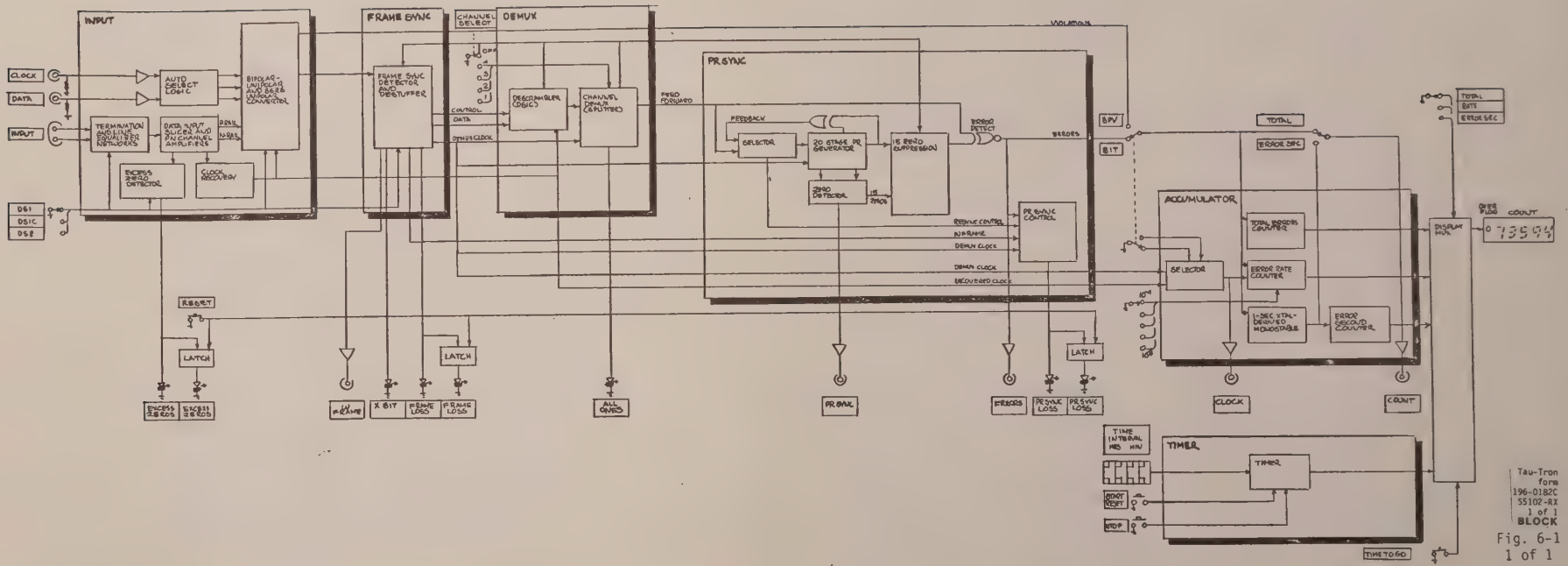
6-8 DISPLAY BOARD ASSEMBLY DRAWING AND SCHEMATIC.

6-9 MOTHERBOARD LOADING DIAGRAM AND WIRING DIAGRAM.

6-10 INTERCONNECT DIAGRAM.

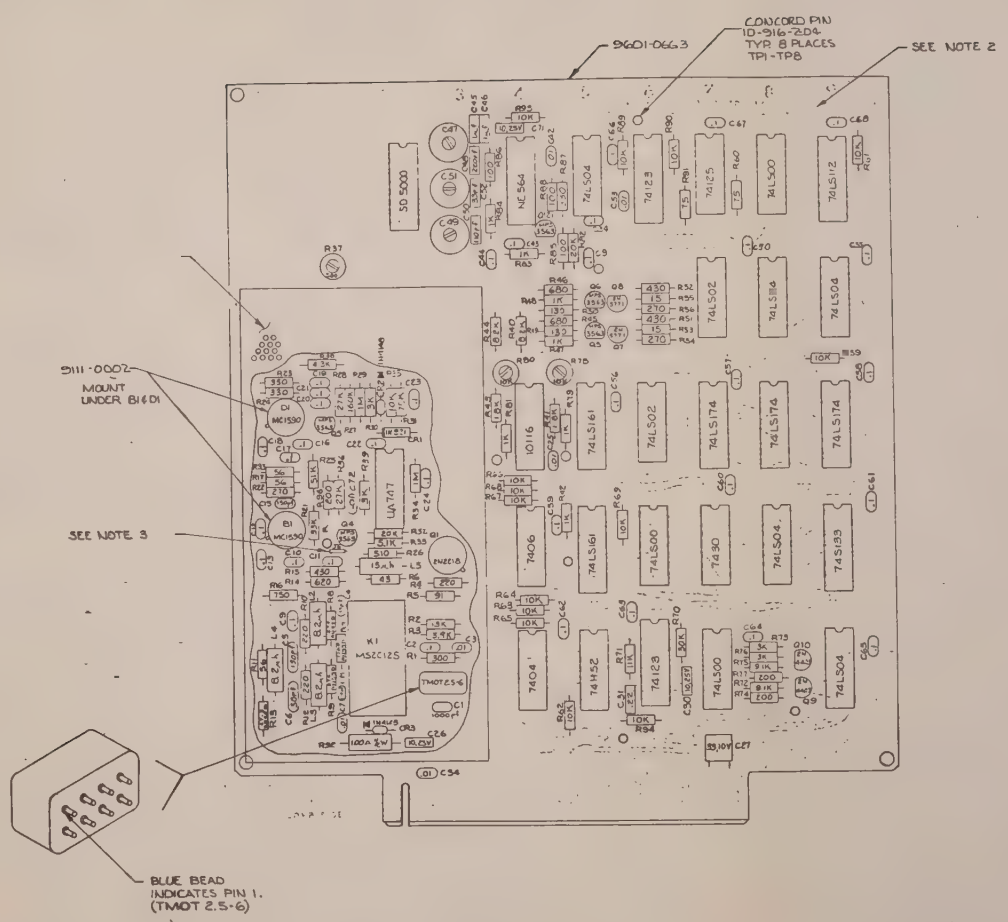
6-11 FRONT-PANEL WIRING DIAGRAM.

6-12 CHASSIS WIRING DIAGRAM.



Tau-Tron form 196-0182C 55102-RX 1 of 1 **BLOCK**

Fig. 6-1
1 of 1



0	ORIGINATED		
1	REV PER DCN 00869		
2	REV PER ECO #00976 DTD 7-30-81		

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTANCE VALUES ARE IN OHMS, ¼W ±5%.
   B. CAPACITANCE VALUES ARE IN MICROFARADS.
2. PLACE A PERMANENT REVISION LEVEL MARK ON THE ASSEMBLY IN THE DESIGNATED AREA.
3. JUMPERS TO BE #24 BUSS WIRE WITH SLEEVING.

C. ATHERTON 1-8-81
B. COOPER 1-13-81
W.E. LITTLE 1-13-81

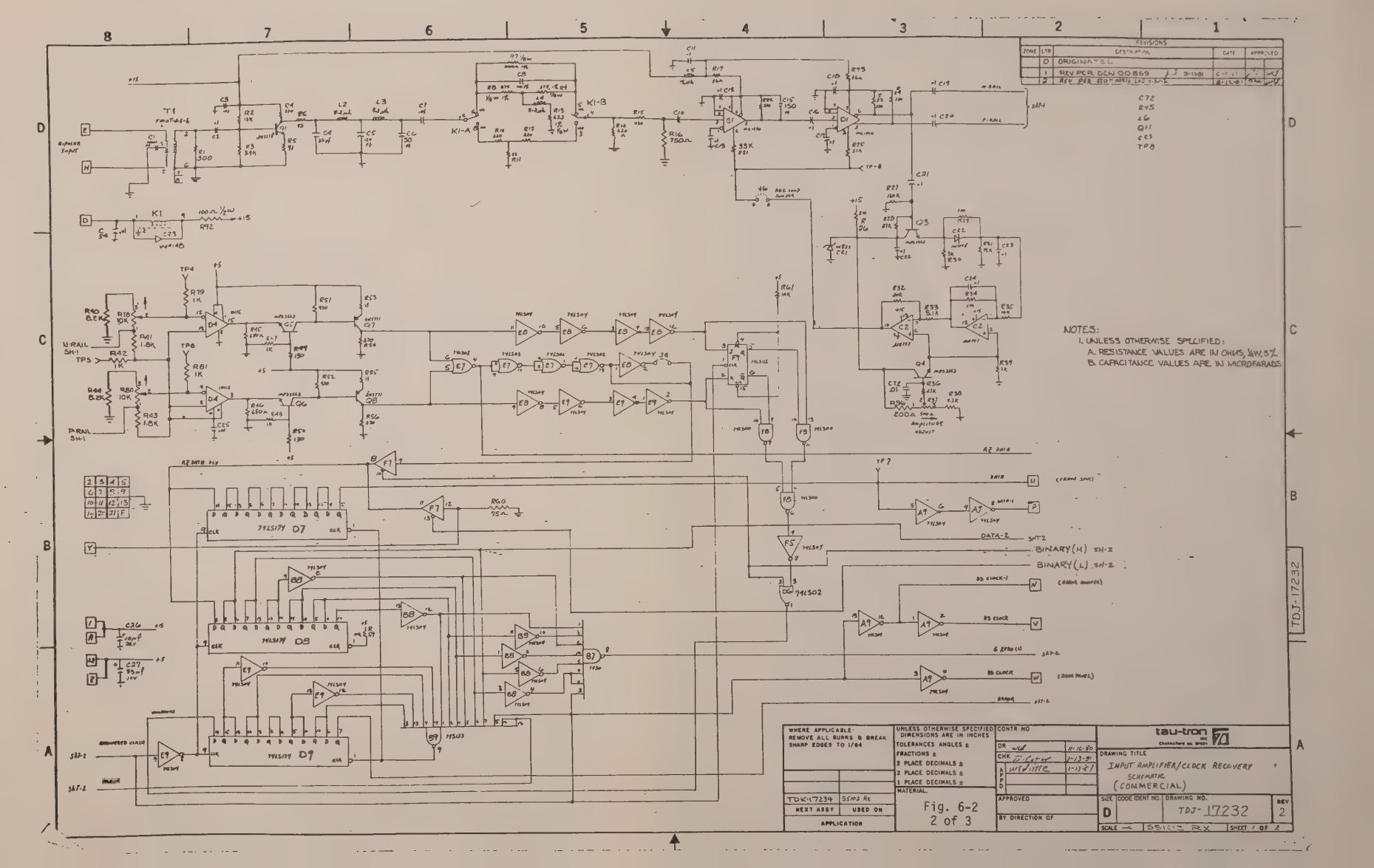
ASSEMBLY
COMMERCIAL
INPUT AMP/CLOCK RECOVERY

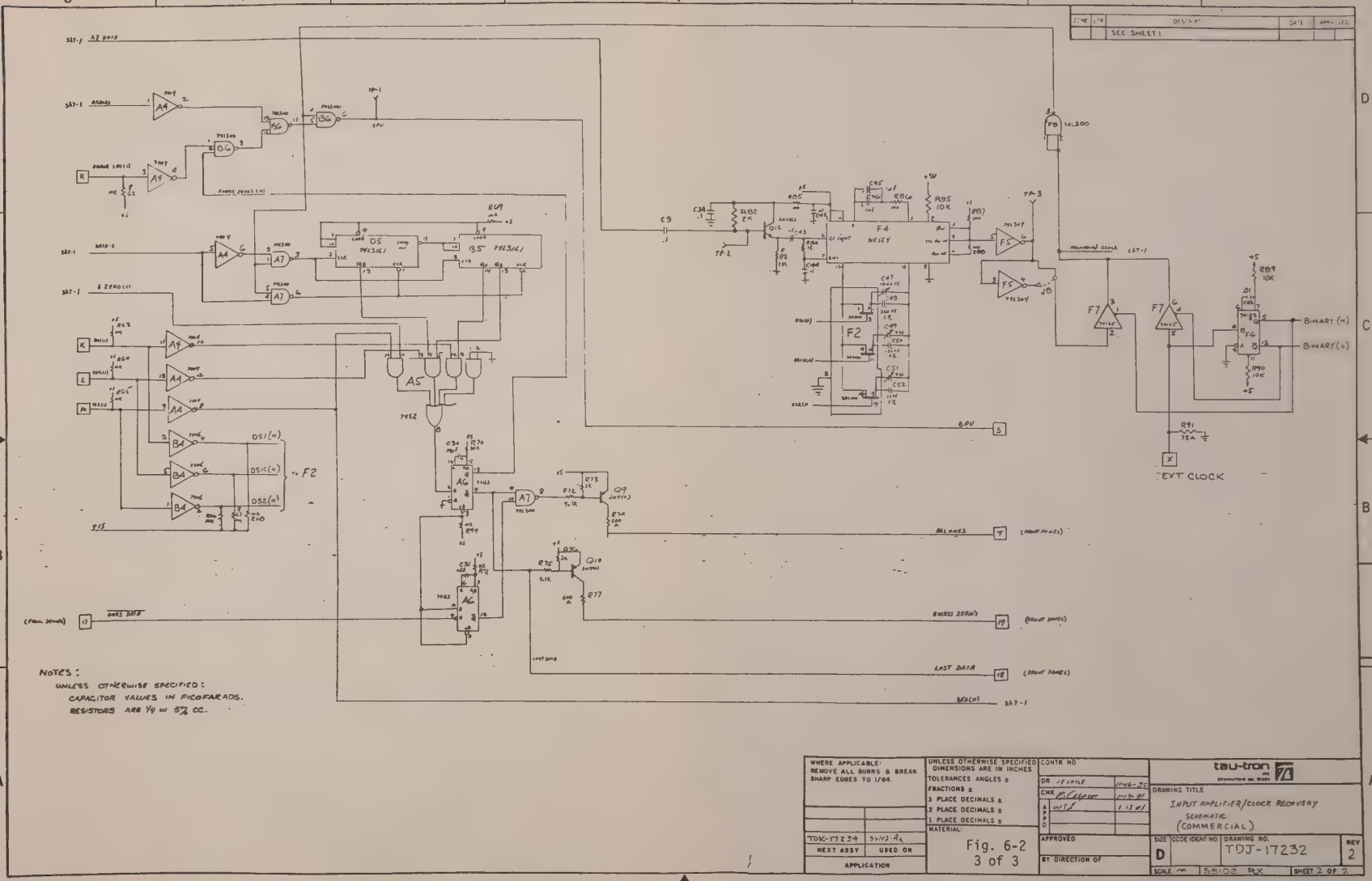
35102 RX

Fig. 6-2
1 of 3

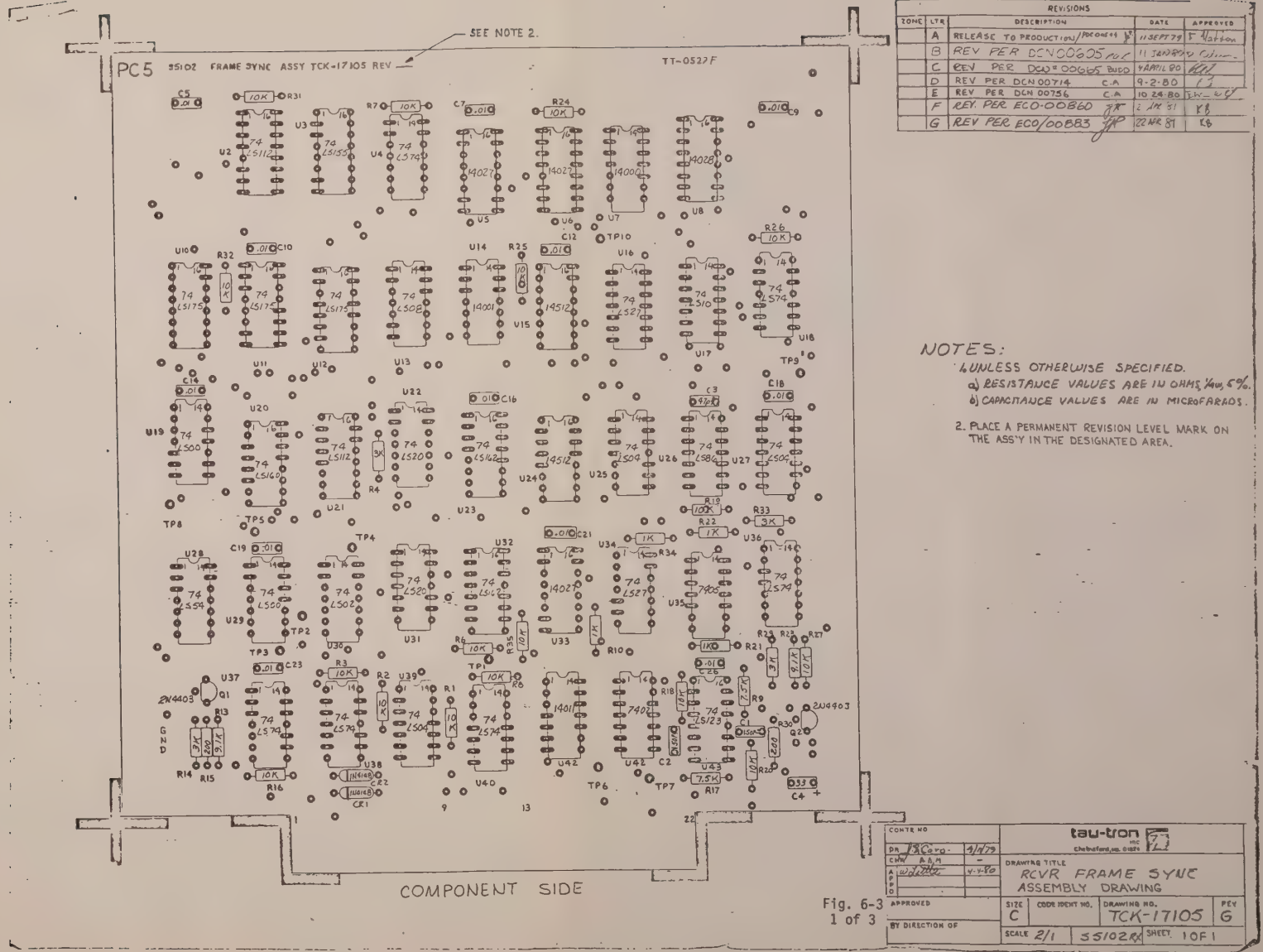
TDK-17234 2

35102 RX


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
0 ORIGINATED
1 REV PER DCN 00869 3-11-81
2 REV PER ECO 0091 DTD 3-30-82
C72
R45
L6
Q11
CR3
TP8
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
A. RESISTANCE VALUES ARE IN OHMS, ¼W, 5%
B. CAPACITANCE VALUES ARE IN MICROFARADS
TDJ-17232
WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ANGLES ±
FRACTIONS ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMALS ±
MATERIAL
CONTR NO
DR
CHK
APPD
APPROVED
BY DIRECTION OF
tau-tron inc
DRAWING TITLE
INPUT AMPLIFIER/CLOCK RECOVERY SCHEMATIC (COMMERCIAL)
SIZE D
CODE IDENT NO.
DRAWING NO. TDJ-17232
REV 2
SCALE —
SHEET 1 OF 2
TDK-17234
NEXT ASSY
USED ON
APPLICATION
Fig. 6-2
2 of 3



WHERE APPLICABLE: REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64.	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± FRACTIONS ± 3 PLACE DECIMALS ± 2 PLACE DECIMALS ± 1 PLACE DECIMALS ± MATERIAL	CONTR NO DR J.E.LITTLE 11-16-72 CHK R.C.CARLSON 11-21-72 APPD W.C.F. 1-13-73 APPROVED BY DIRECTION OF	tau-tron DRAWING TITLE INPUT AMPLIFIER/CLOCK RECOVERY SCHEMATIC (COMMERCIAL)
TDK-17234 / 55102-RX NEXT ASSY / USED ON APPLICATION	Fig. 6-2 3 of 3		SIZE D / CODE IDENT NO / DRAWING NO. TDJ-17232 / REV 2 SCALE — / 55102 RX / SHEET 2 OF 2



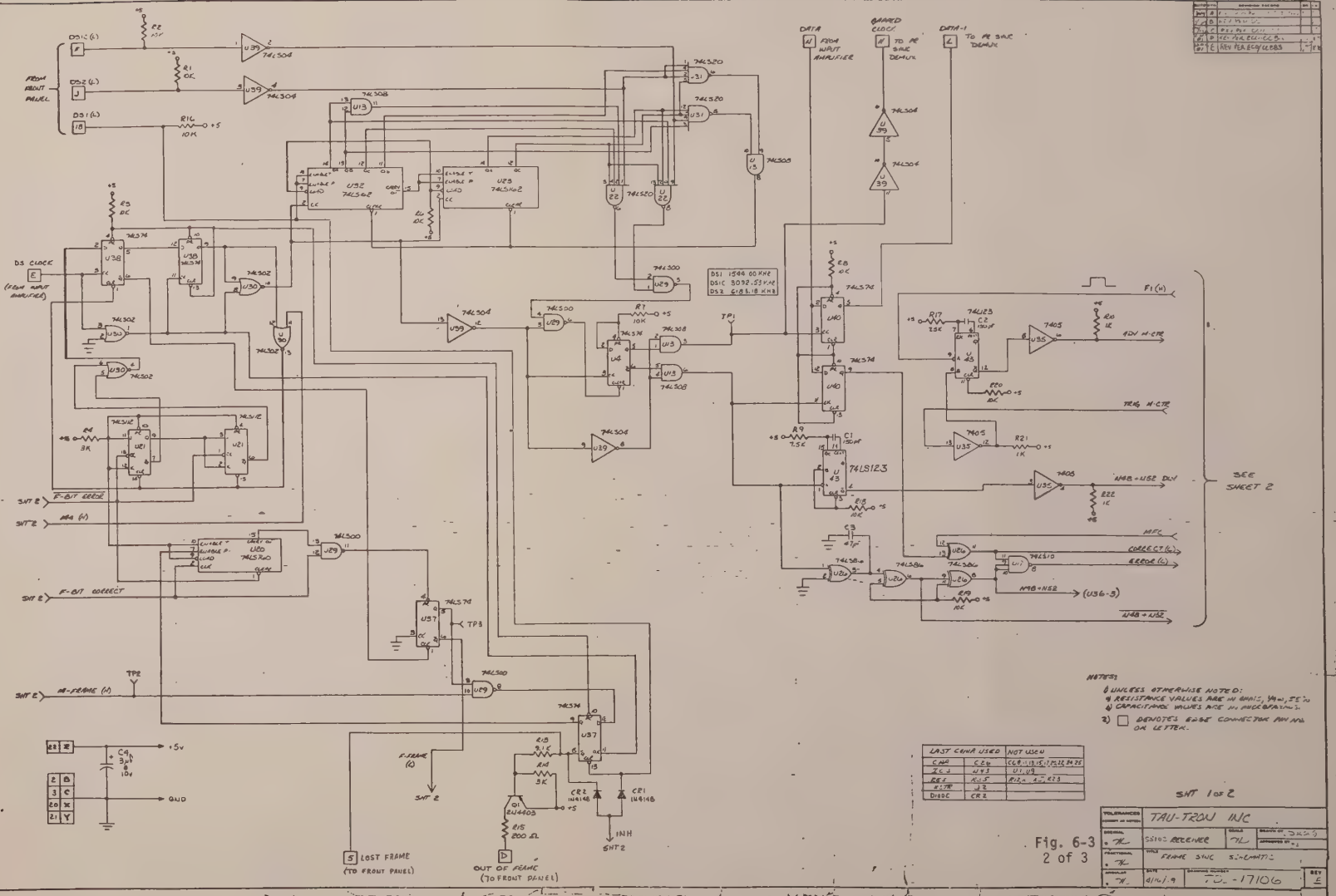
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	RELEASE TO PRODUCTION/PROCESS	11 SEPT 79	[illegible]
	B	REV PER DCN00605	11 JANUARY 80	[illegible]
	C	REV PER DCN=00665	4 APRIL 80	[illegible]
	D	REV PER DCN 00714 C.A	9-2-80	[illegible]
	E	REV PER DCN 00756 C.A	10 24 80	[illegible]
	F	REV. PER ECO-00860	2 JAN 81	KB
	G	REV PER ECO/00883	22 MAR 81	KB

NOTES:

1. UNLESS OTHERWISE SPECIFIED.
   a) RESISTANCE VALUES ARE IN OHMS, ¼w, 5%.
   b) CAPACITANCE VALUES ARE IN MICROFARADS.
2. PLACE A PERMANENT REVISION LEVEL MARK ON THE ASS'Y IN THE DESIGNATED AREA.

CONTR NO		tau-tron INC Chelmsford, MA. 01824
DR J.Cara	3/1/79	
CHK A.A.M	—	
APPD [illegible]	4-4-80	
DRAWING TITLE		RCVR FRAME SYNC ASSEMBLY DRAWING
APPROVED		SIZE C / CODE IDENT NO. / DRAWING NO. TCK-17105 / REV G
BY DIRECTION OF		SCALE 2/1 / 35102 / SHEET 1 OF 1

Fig. 6-3
1 of 3


DS1(L)
DS2(L)
DS3(L)
FROM FRONT PANEL
DS CLOCK
(FROM WAVE AMPLIFIER)
DATA
FROM WAVE AMPLIFIER
BOARD CLOCK
TO PE SYNC DEMUX
DATA-1
TO PE SYNC DEMUX
DS1 1544.00 KHZ
DS1C 3092.53 KHZ
DS2 6185.18 KHZ
F1(H)
ADJ M-CTR
TRIG M-CTR
M4B+M52 DLY
M4B+M52
M4B+M52 (U36-3)
M4B (H)
M4
M52
M5
M5C
CORRECT(L)
ERROR(L)
SHT E
F-BIT ERROR
F-BIT CORRECT
RE-FRAME (H)
TP2
TP3
TP1
F-FRAME (L)
+5V
GND
LOST FRAME
(TO FRONT PANEL)
OUT OF FRAME
(TO FRONT PANEL)
INH
SHT 2
SEE SHEET 2
74LS374
74LS300
74LS123
74LS10
74LS86
74LS38
74LS08
74LS02
74LS04
74LS20
74LS08
74LS32
74LS74
74LS00
74LS157
74LS163
74LS90
74LS192
74LS193
74LS283
74LS85
74LS280
74LS151
74LS153
74LS251
74LS257
74LS258
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74LS732
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74LS734
74LS735

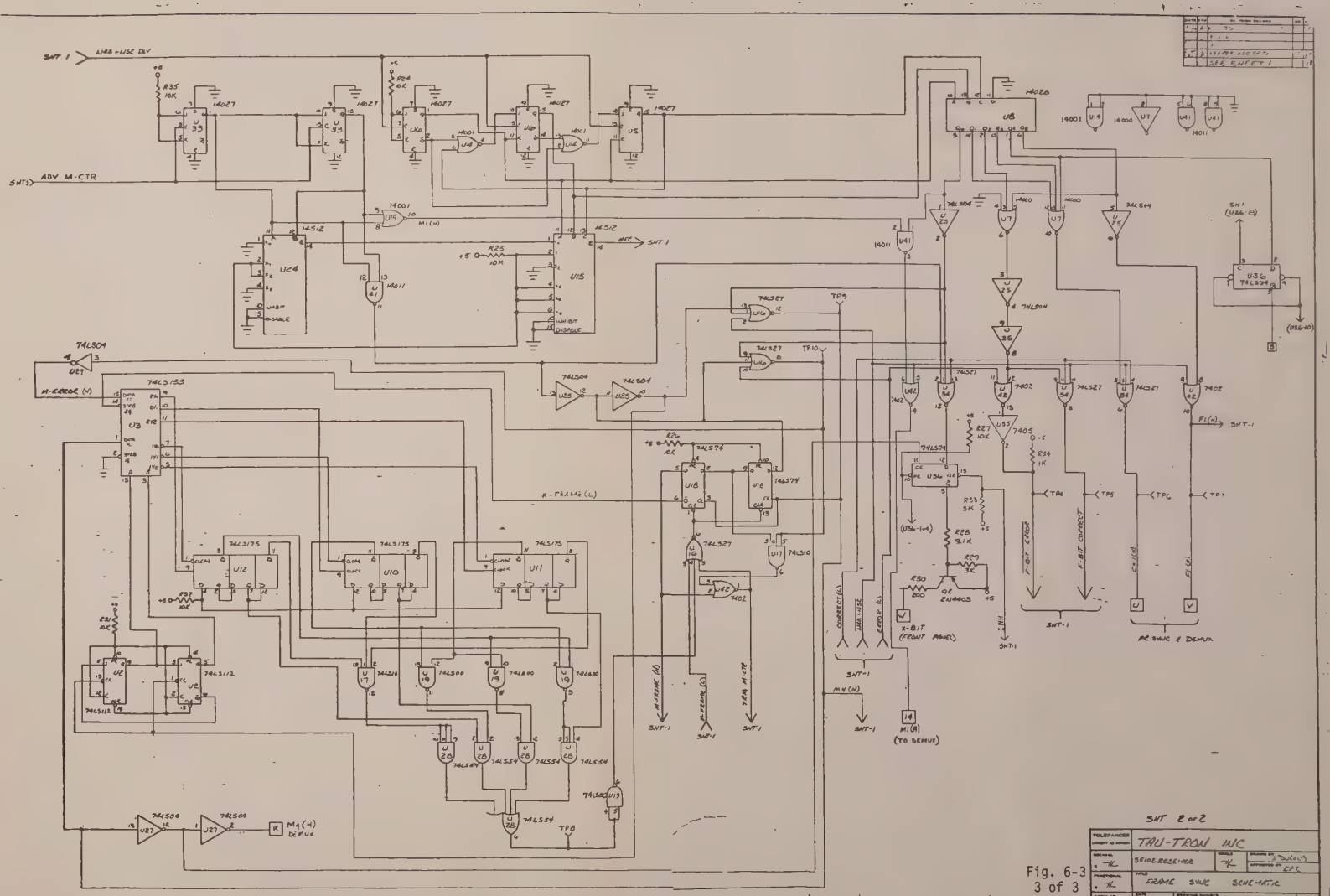
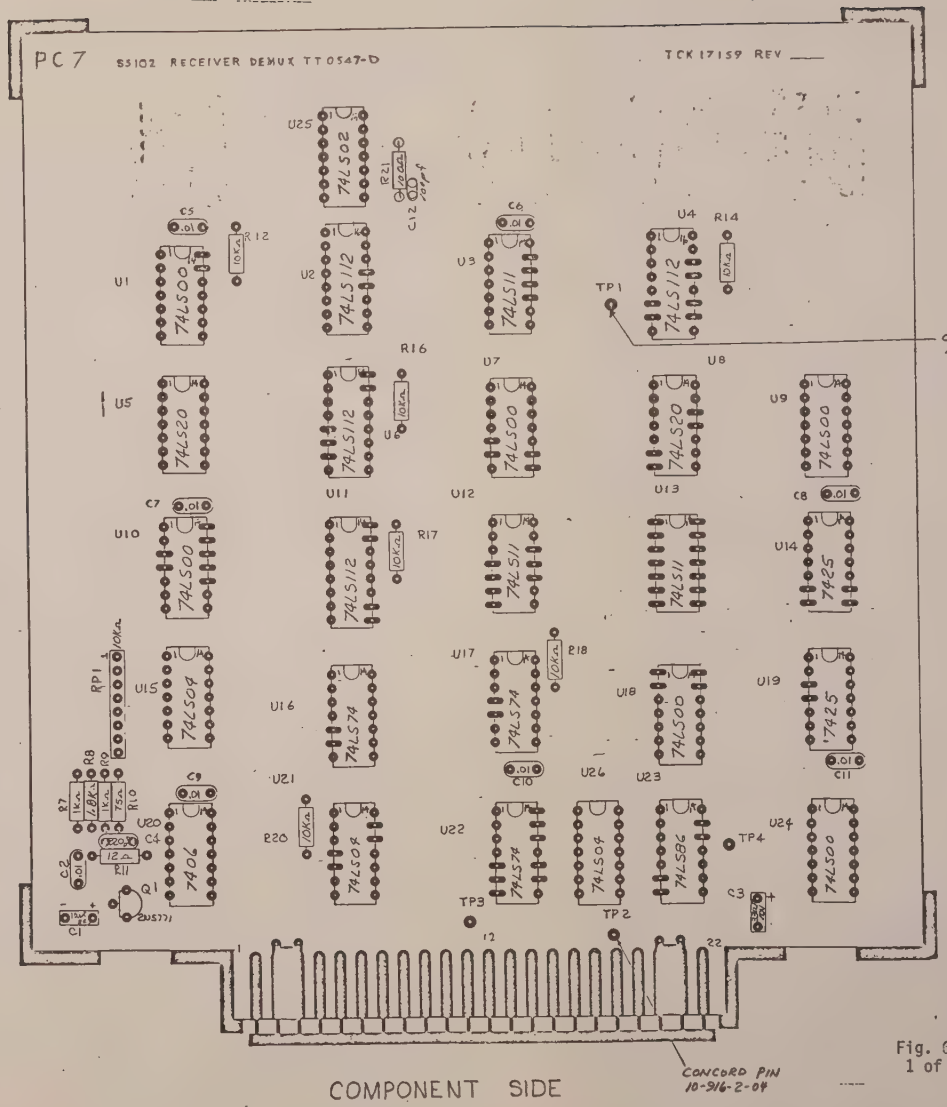

SHT 1
ADV M-CTR
SHT 2
M-ERROR (H)
M-FRAME (L)
SHT 2 of 2
TAU-TRON INC
SEIOR RECEIVER
FRAME SYNC SCHEMATIC
TDJ-17106
4/10/79

Fig. 6-3
3 of 3



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	RELEASED TO PROD. PER PDC00544	9-5-79	
	B	REV PER DCN 00605 DGD	1-11-80	
	C	ADDED ITEM 33, 2 PLACES CHANGED RB FROM 82E TO 10K	4-8-80	AAM
	D	REV. PER DCN NO. 00673	23 APR 80	
	E	REV PER DCN 00839	14-17-81	23 APR 81 GAC KB

NOTES:
1. UNLESS OTHERWISE SPECIFIED
   A) RESISTANCE VALUES ARE IN OHMS, 1/4 W, ±5%.
   B) CAPACITANCE VALUES ARE IN MICROFARADS.

Fig. 6-4
1 of 2

CONTR NO.		tektron inc.	
DR W MCKENNA 4-24-79			
CHK AAM		DRAWING TITLE	RECEIVER DEMUX ASSEMBLY DRAWING
APPROVED		SIZE C	CODE IDENT NO.
BY DIRECTION OF		DRAWING NO. TCK-17159	REV E
		SCALE 2/1	55102 SHEET 1 OF 1

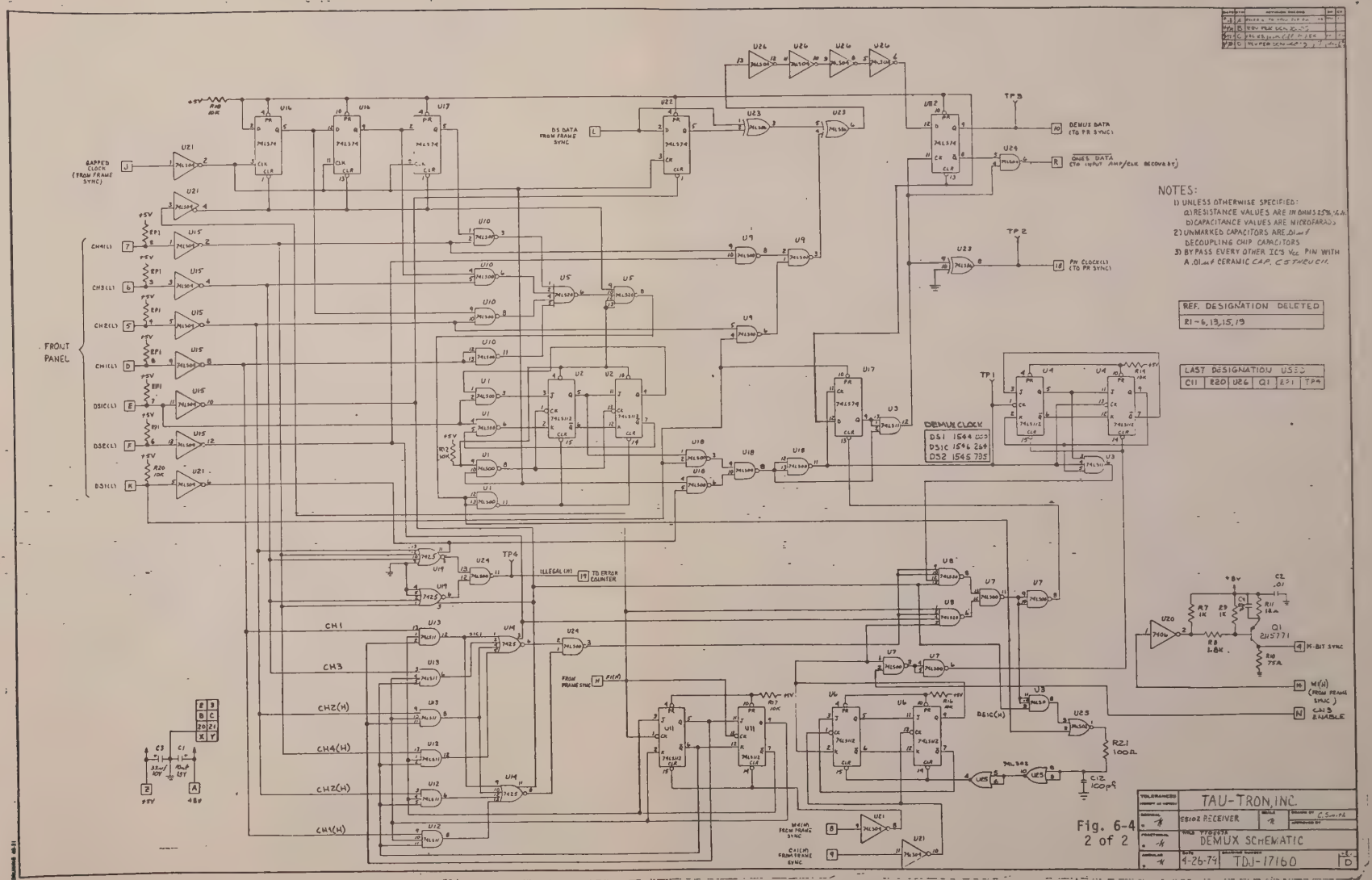
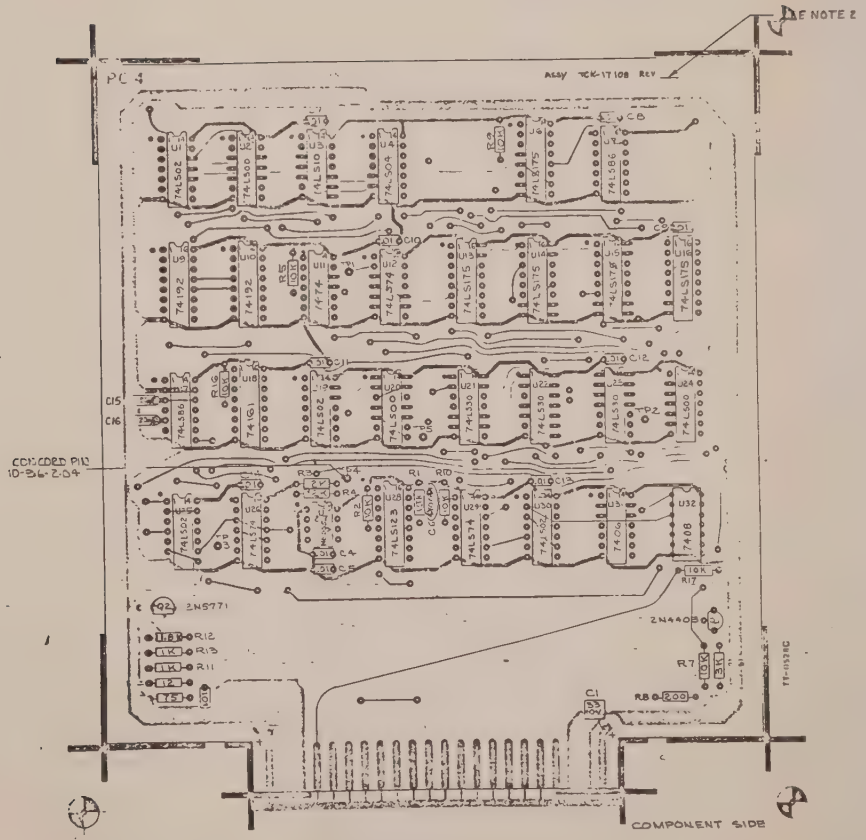

NOTES:
1) UNLESS OTHERWISE SPECIFIED:
a) RESISTANCE VALUES ARE IN OHMS ±5%, ¼ W.
b) CAPACITANCE VALUES ARE MICROFARADS
2) UNMARKED CAPACITORS ARE .01μF DECOUPLING CHIP CAPACITORS
3) BY PASS EVERY OTHER IC'S Vcc PIN WITH A .01μF CERAMIC CAP. C5 THRU C11.
REF. DESIGNATION DELETED
C1 - 6, 13, 15, 19
LAST DESIGNATION USED
C11 | R20 | U26 | Q1 | E21 | TP4
DEMUX CLOCK
DS1 1544 003
DS1C 1545 269
DS2 1545 705
FRONT PANEL
GAPPED CLOCK (FROM FRAME SYNC)
DS DATA FROM FRAME SYNC
DEMUX DATA (TO PR SYNC)
ONES DATA (TO INPUT AMP/CLK RECOVERY)
PW CLOCK(L) (TO PR SYNC)
TD ERROR COUNTER
ILLEGAL (H)
FROM FRAME SYNC
W(H) (FROM FRAME SYNC)
CH3 ENABLE
M-BIT SYNC
CH1
CH3
CH2(H)
CH4(H)
CH2(H)
CH4(H)
DS1C(H)
W(H) FROM FRAME SYNC
C4(H) FROM FRAME SYNC
TAU-TRON, INC.
8810Z RECEIVER
DEMUX SCHEMATIC
4-26-74
TDJ-17160
D

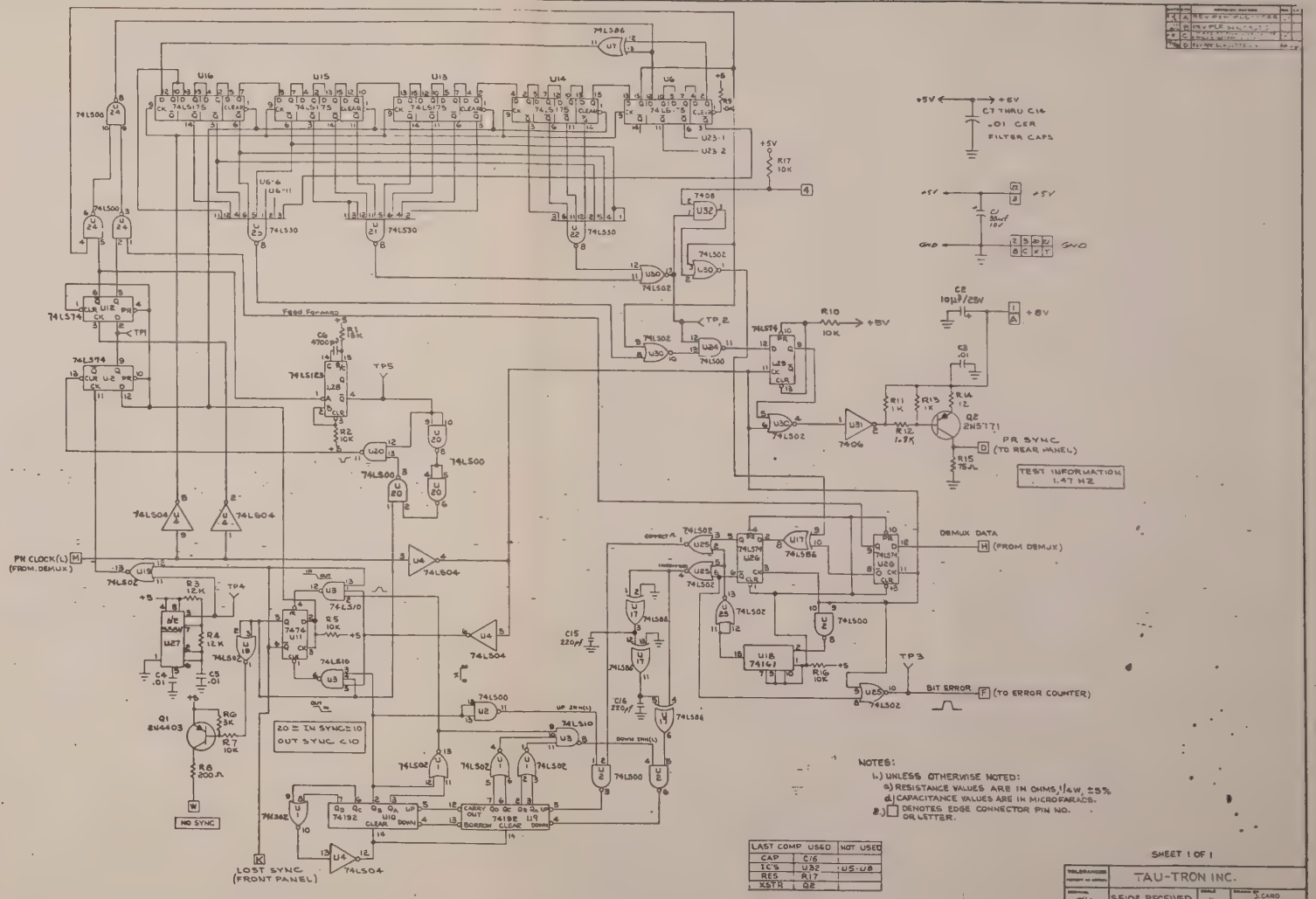
Fig. 6-4
2 of 2



NOTES:
1. UNLESS OTHERWISE SPECIFIED,
   A) RESISTANCE VALUES ARE IN OHMS, 1 5% ¼w.
   B) CAPACITANCE VALUES ARE IN MICROFARADS.
2. PLACE A PERMANENT REVISION LEVEL MARK ON THE ASSEMBLY IN THE DESIGNATED AREA.

Fig. 6-5
1 of 2

	TAJ-007	
	TITLE: ASSEMBLY DRAWING PR SYNC	
	D TDK-17108	REV D
	SCALE 2/1 SIZE	SHEET



NOTES:
1.) UNLESS OTHERWISE NOTED:
a) RESISTANCE VALUES ARE IN OHMS, 1/4W, ±5%
d) CAPACITANCE VALUES ARE IN MICROFARADS.
2.) □ DENOTES EDGE CONNECTOR PIN NO. OR LETTER.

LAST COMP USED		NOT USED
CAP	C16	
IC'S	U32	U5-U8
RES	R17	
XSTR	Q2	

SHEET 1 OF 1

TAU-TRON INC.

S5102 RECEIVER

PR SYNC SCHEMATIC

5-8-79

TDJ-17109 REV D

Fig. 6-5
2 of 2

A	ORIGINATED	JP 3-21-80		
B	PER ECO 00679	CS 4-25-80	6-20-80	
C	PER ECO 00701	CS 6-9-80	6-11-80	
D	REV. PER ECO/00971			

NOTES:
1. UNLESS OTHERWISE SPECIFIED
   A) RESISTOR VALUES ARE IN OHMS, 1/4 W, 5%.
   B) CAPACITOR VALUES ARE IN MICROFARADS.
2. * INDICATES SELECT VALUE AT TEST.

JBST 3-21-80
R.C. NILL 3-24-80
W. Whitte 3-24-80

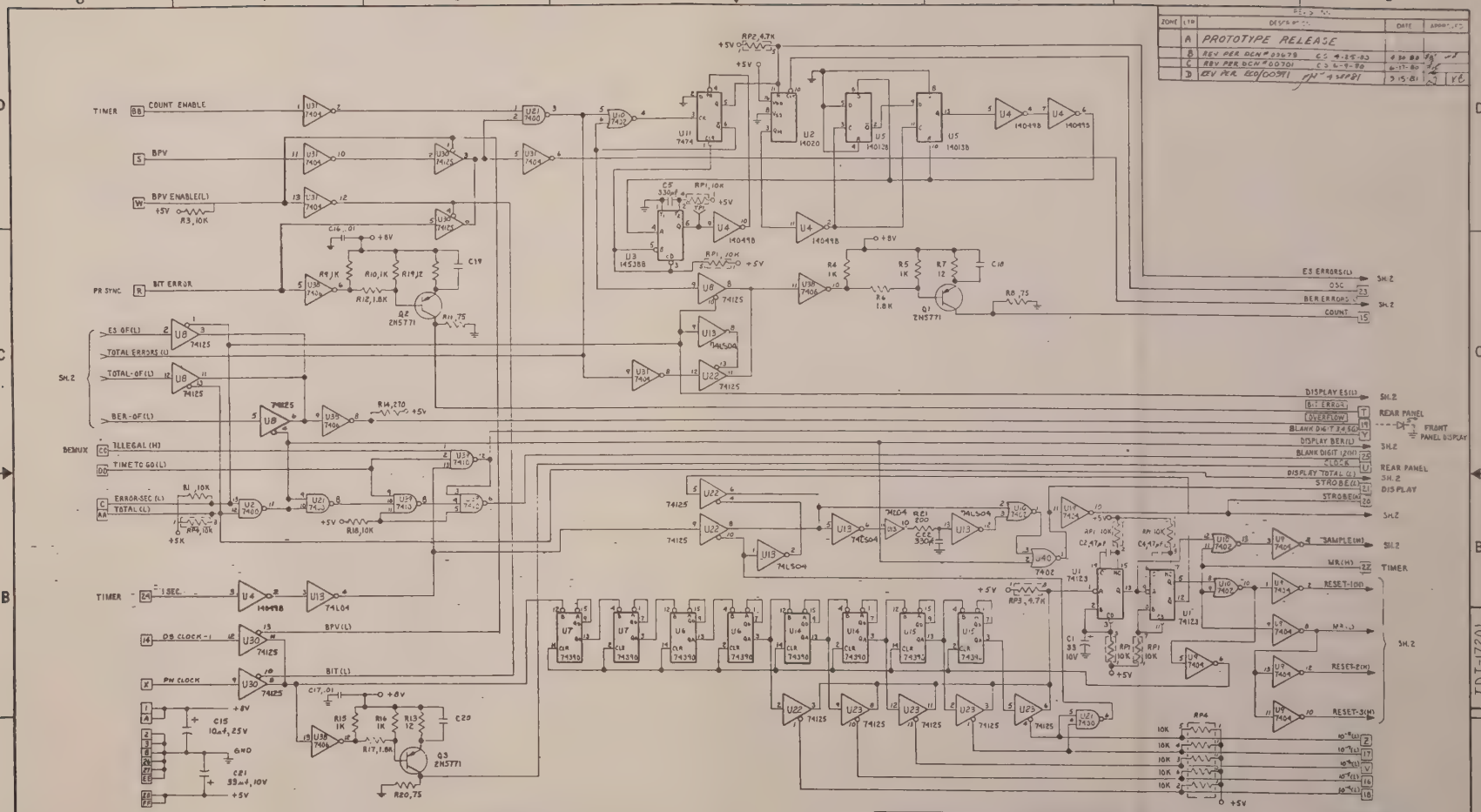
ERROR ACCUMULATOR ASSEMBLY

55102 AX

Fig. 6-6 1 of 3

TDK-17202 D

2/1 55102 AX



ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PROTOTYPE RELEASE		
	B	REV PER DCN #03679 CS	4-25-80	
	C	REV PER DCN #00701 CS	6-17-80	
	D	REV PER ECO 00591	3-15-81	

LAST REFDES USED	NOT USED
Q3	
C22	
U40	
RE1	
RP10	
TP1	

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A) RESISTANCE VALUES ARE IN OHMS, ¼ W, ± 5%.
   B) CAPACITANCE VALUES ARE IN MICROFARADS.
2. JUMPER TO BE INSTALLED IN TEST PER TEST PROCEDURE.

REFERENCE DRAWINGS:
ASSEMBLY: TDK-17202
FABRICATION: TDS-17203

WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
FRACTIONS ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMALS ±
MATERIAL

CONTR NO
DR C. SMITH 2-7-80
CHK T. T. T 2-19-80
APP'D 4-11-80

NEXT ASSY | USED ON
SS102 REVR
APPLICATION

Fig. 6-6
2 of 3

APPROVED
BY DIRECTION OF

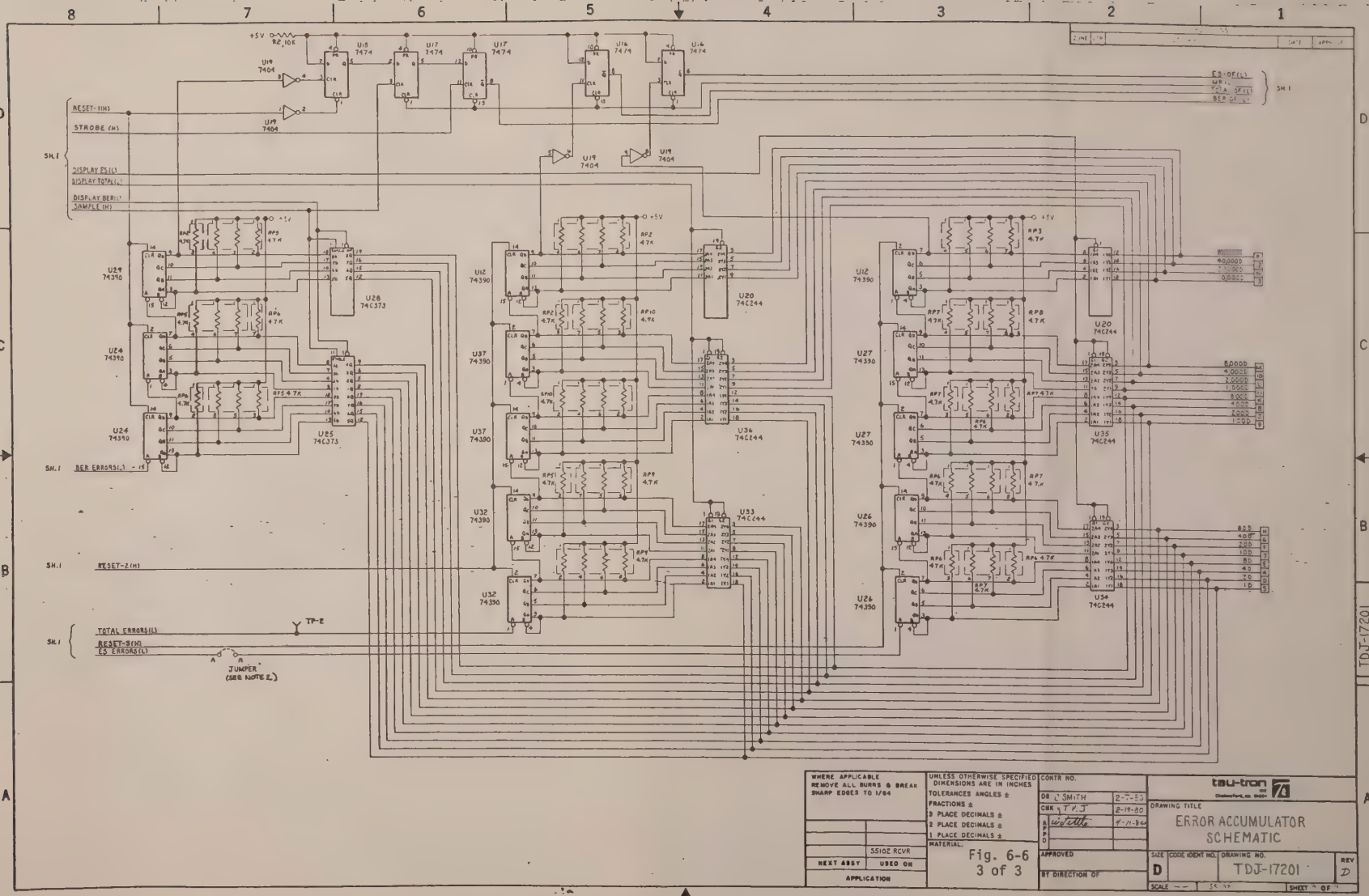
tau-tron inc. Chelmsford, Mass. 01824

DRAWING TITLE
ERROR ACCUMULATOR SCHEMATIC

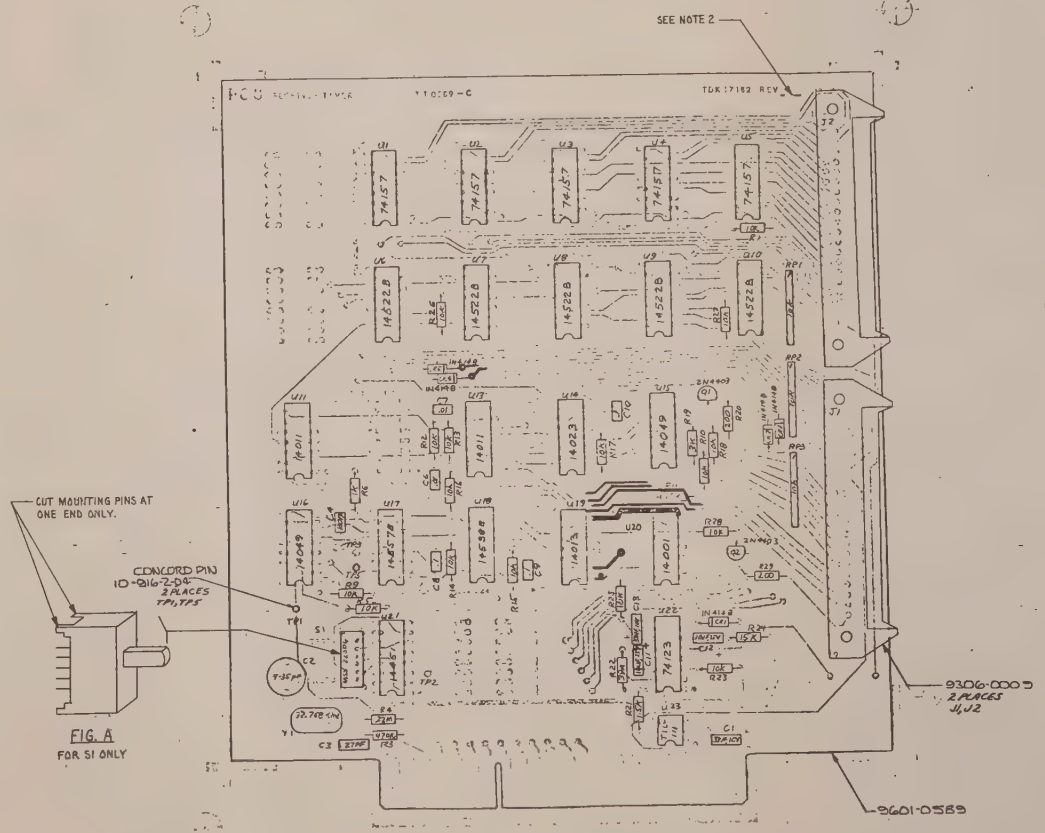
SIZE	CODE IDENT NO	DRAWING NO.	REV
D		TDJ-17201	D

SCALE — SHEET

TDJ-17201



WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± FRACTIONS ± 3 PLACE DECIMALS ± 2 PLACE DECIMALS ± 1 PLACE DECIMALS ± MATERIAL:	CONTR NO. DR L SMITH 2-7-83 CHK T.P.J 2-19-83 APPD wjstitt 4-11-84 APPROVED BY DIRECTION OF	tau-tron DRAWING TITLE ERROR ACCUMULATOR SCHEMATIC
5510Z RCVR NEXT ASSY USED ON APPLICATION	Fig. 6-6 3 of 3		SIZE D · CODE IDENT NO. · DRAWING NO. TDJ-17201 · REV D SCALE — · SHEET — OF —



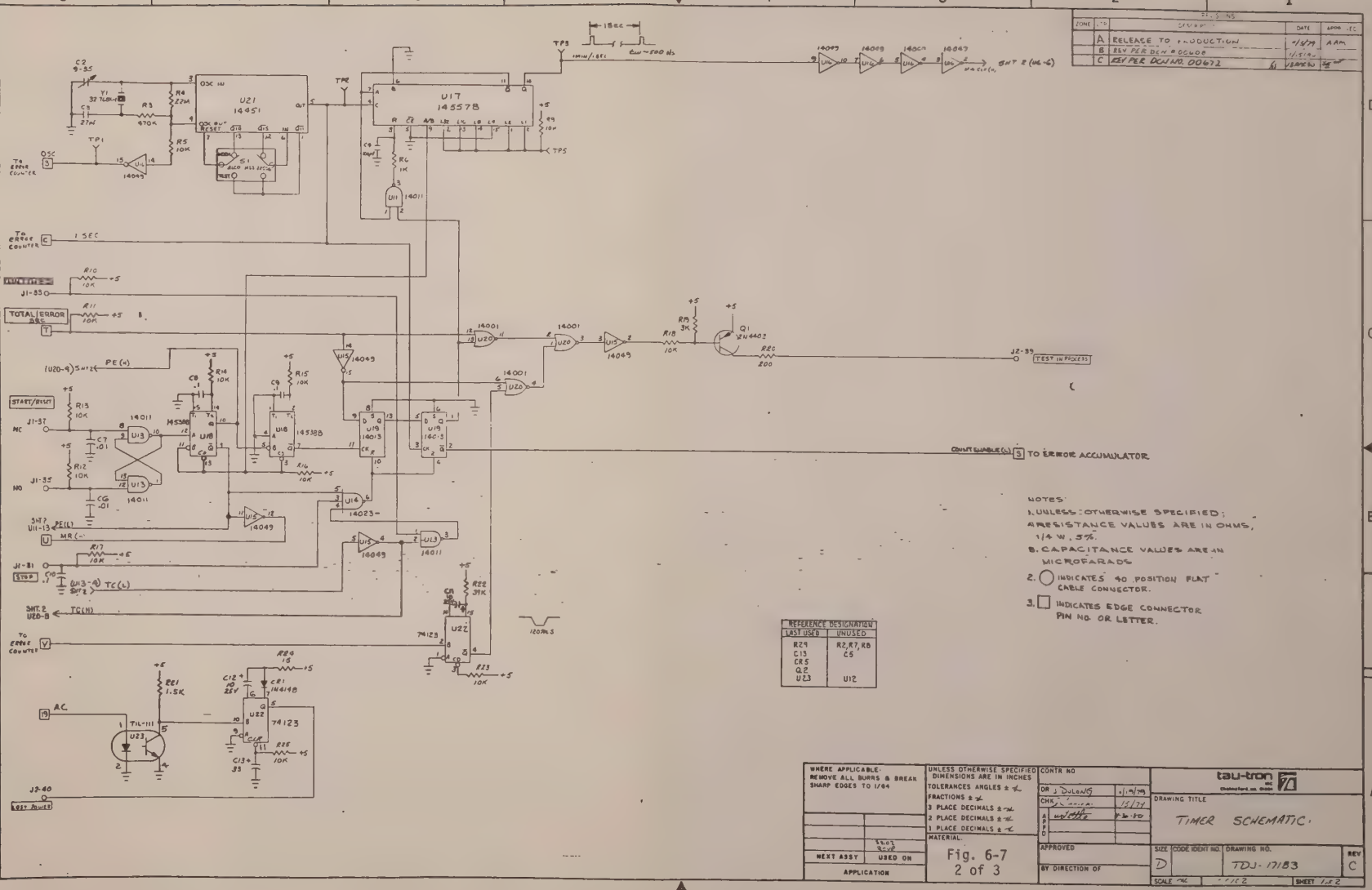
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A) RESISTANCE VALUES ARE IN OHMS, 1/4 W, ± 5%
   B) CAPACITANCE VALUES ARE IN MICROFARADS.
2. PLACE A PERMANENT REVISION LEVEL MARK ON THE ASSEMBLY IN THE DESIGNATED AREA.

A	RELEASE TO PRODUCTION		AAA
B	REV PER DCN 00609		
C	REV PER DCN NO 00672		
D	REV PER DCN 00749		

RECEIVER TIMER ASSEMBLY DRAWING

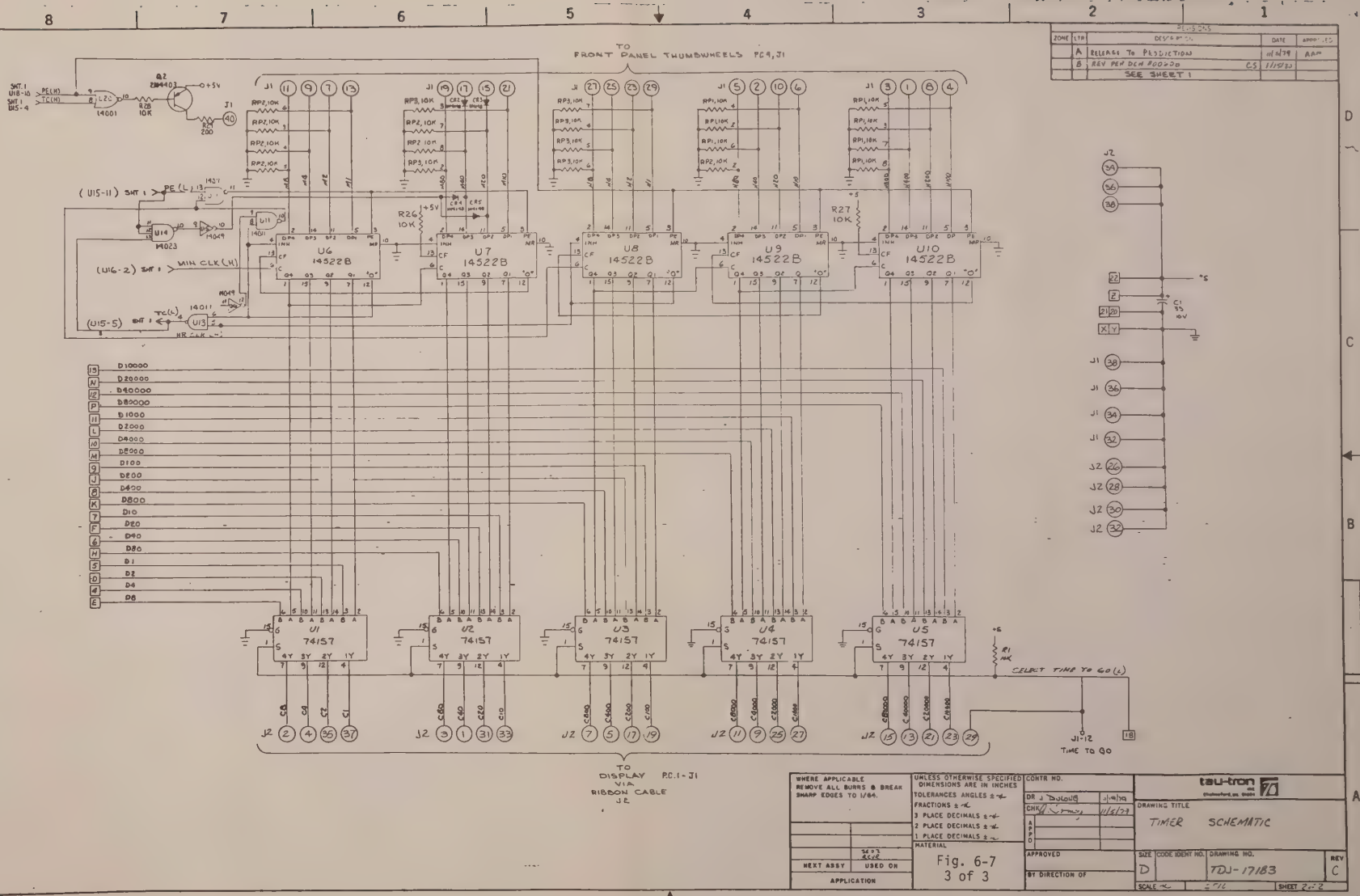
TDK-17182 D

Fig. 6-7
1 of 3



ZONE	LTR	DESCRIPTION	DATE	APPD
	A	RELEASE TO PRODUCTION	4/5/79	AAM
	B	REV PER DCN # 00600	11/5/79	
	C	REV PER DCN NO. 00672	1/22/80	

WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES; TOLERANCES ANGLES ± ½; FRACTIONS ± 1/64; 3 PLACE DECIMALS ± .005; 2 PLACE DECIMALS ± .01; 1 PLACE DECIMALS ± .1	CONTR NO	tau-tron, Stamford, Conn.
	MATERIAL	DR J DuLong 1/19/79; CHK [illegible] 1/5/79; APPD [illegible] 2-5-80	DRAWING TITLE: TIMER SCHEMATIC
NEXT ASSY / USED ON	Fig. 6-7 2 of 3	APPROVED	SIZE D; CODE IDENT NO.; DRAWING NO. TDJ-17183; REV C
APPLICATION		BY DIRECTION OF	SCALE NONE; SHEET 1 of 2



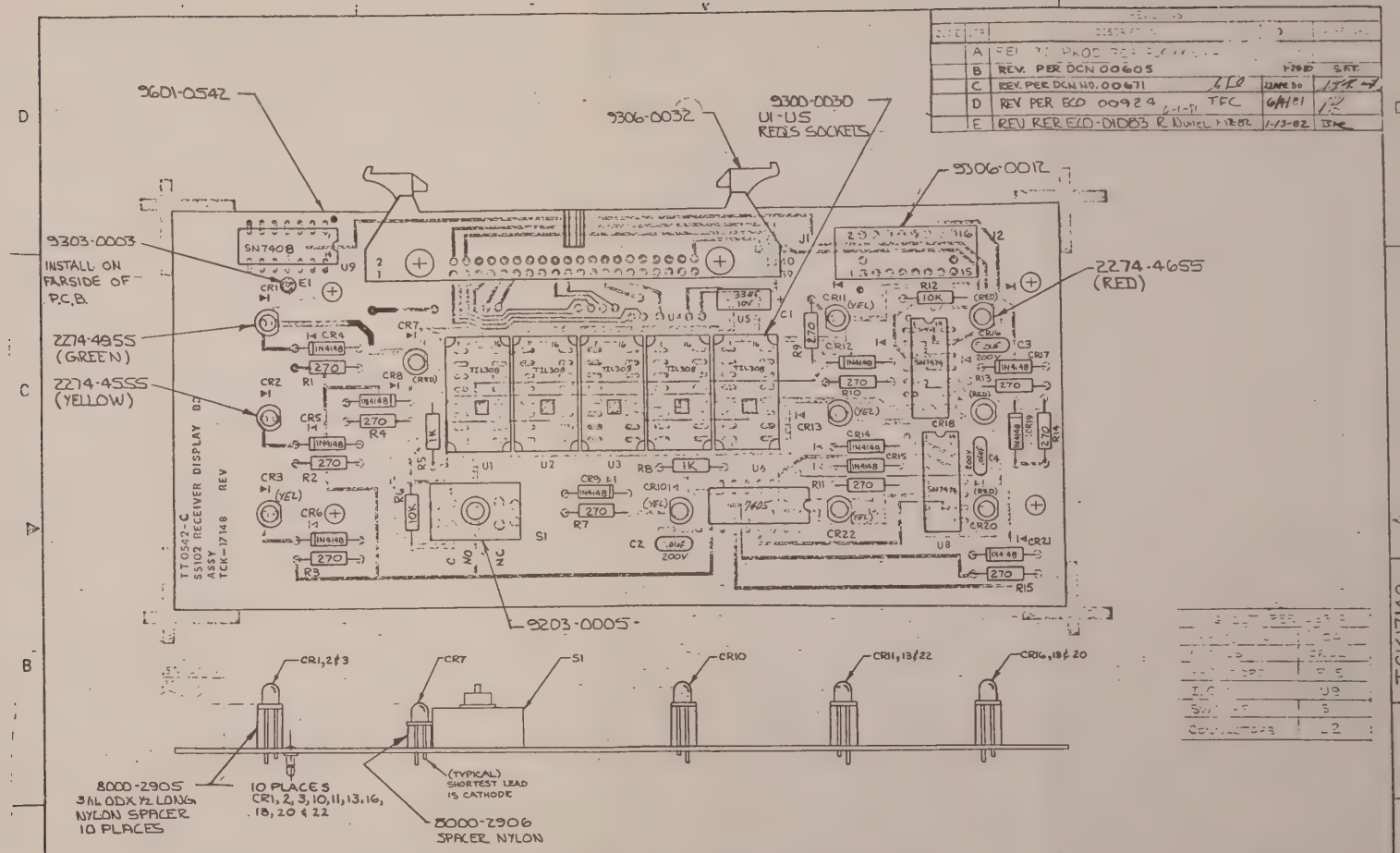
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	RELEASE TO PRODUCTION	11/6/79	AAM
	B	REV PER DCN #00220	11/5/80	
		SEE SHEET 1		

DR J DUDONIS	11/6/79
CHK	11/6/79
APPD	
APPROVED	
BY DIRECTION OF	

DRAWING TITLE	TIMER SCHEMATIC
SIZE	D
CODE IDENT NO.	
DRAWING NO.	TDJ-17183
REV	C
SCALE	3/16
SHEET	2 of 2

NEXT ASSY	USED ON
APPLICATION	

Fig. 6-7
3 of 3



A	PER TC PROD REL [illegible]		
B	REV. PER DCN 00605	[illegible]	
C	REV. PER DCN NO. 00671	[illegible]	
D	REV PER ECO 00924	TEC	6/4/81
E	REV PER ECO-01083 R1	[illegible]	1-13-82

1. UNLESS OTHERWISE SPECIFIED, ALL RESISTORS ARE IN OHMS, 1/4W, ±5%.

NOTES:

WHERE APPLICABLE
REMOVE ALL BURRS & BREAK
SHARP EDGES TO 1/64

	S5102 Rx
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
FRACTIONS ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMALS ±
MATERIAL

Fig. 6-8
1 of 2

CONTR NO.

DR	J FLETCHER	10/12/79
CHK	[illegible]	12/19/79
APPD	[illegible]	1-30-80

APPROVED

BY DIRECTION OF

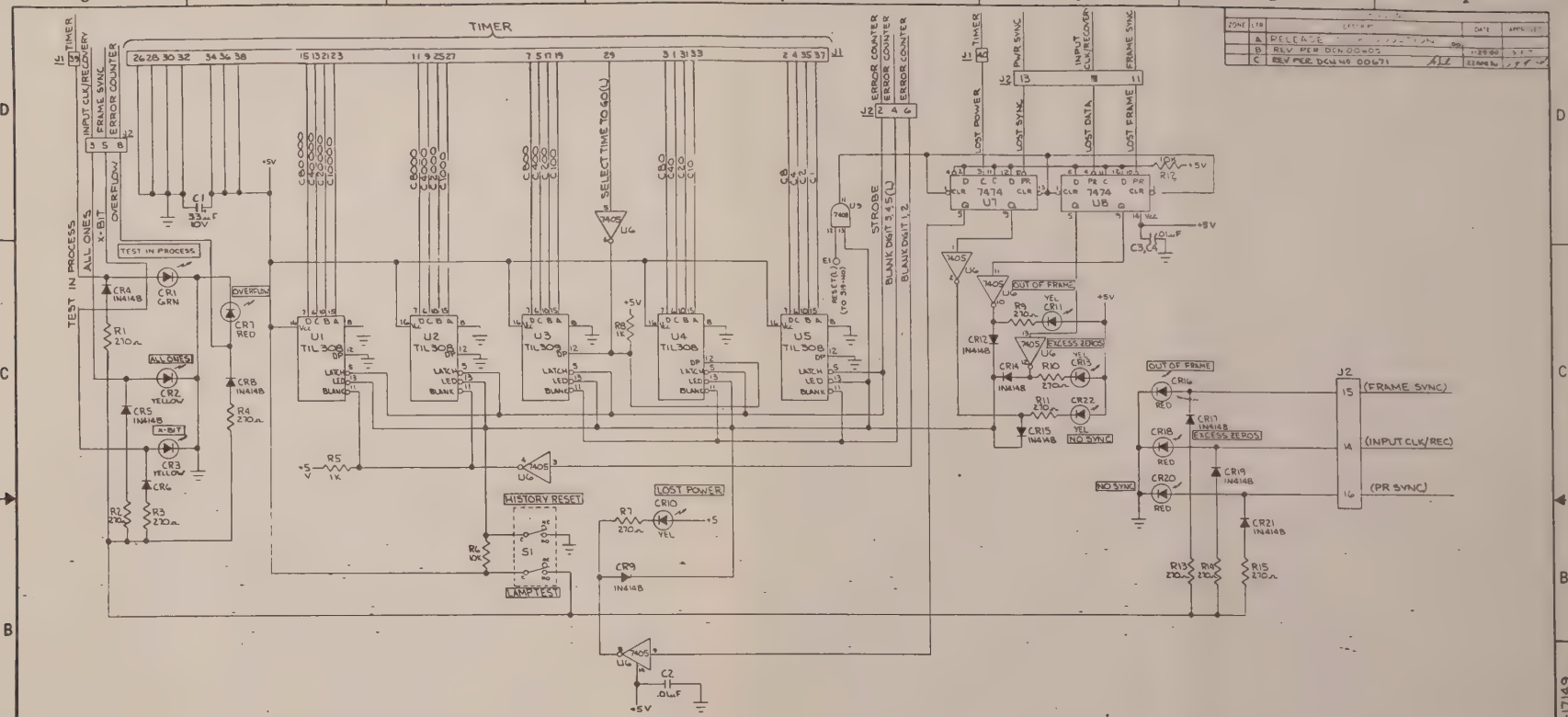
tau-tron inc
Chelmsford, MA 01824

DRAWING TITLE
P.C. ASSEMBLY
S5102, RECEIVER DISPLAY BOARD
(COMPONENT SIDE)

SIZE	CODE IDENT NO	DRAWING NO.	REV
C		TCK-17148	E

SCALE 2/1 | S5102 Rx | SHEET 1 OF 1

TCK-17148



NOTES:

1. RESISTORS ARE ¼W, ±5% CARBON
2. J1[4] INDICATES 16 PIN FLAT RIBBON CONNECTOR AND CONDUCTOR NUMBER.
3. J2[4] INDICATES 40PIN FLAT RIBBON CABLE CONNECTOR AND CONDUCTOR NUMBER.

ZONE	LTR	REVISIONS	DATE	APPROVED
	A	RELEASE		
	B	REV PER DCN 00605	1-28-80	
	C	REV PER DCN 40 00671	6NOV79	

WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ANGLES ±
FRACTIONS ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMALS ±
MATERIAL:

CONTR NO
DR D OLIVER 6NOV79
CHK — 11-28-79
APPD [illegible] 12-3-79
APPROVED
BY DIRECTION OF

NEXT ASSY: S5102-RX
USED ON: APPLICATION

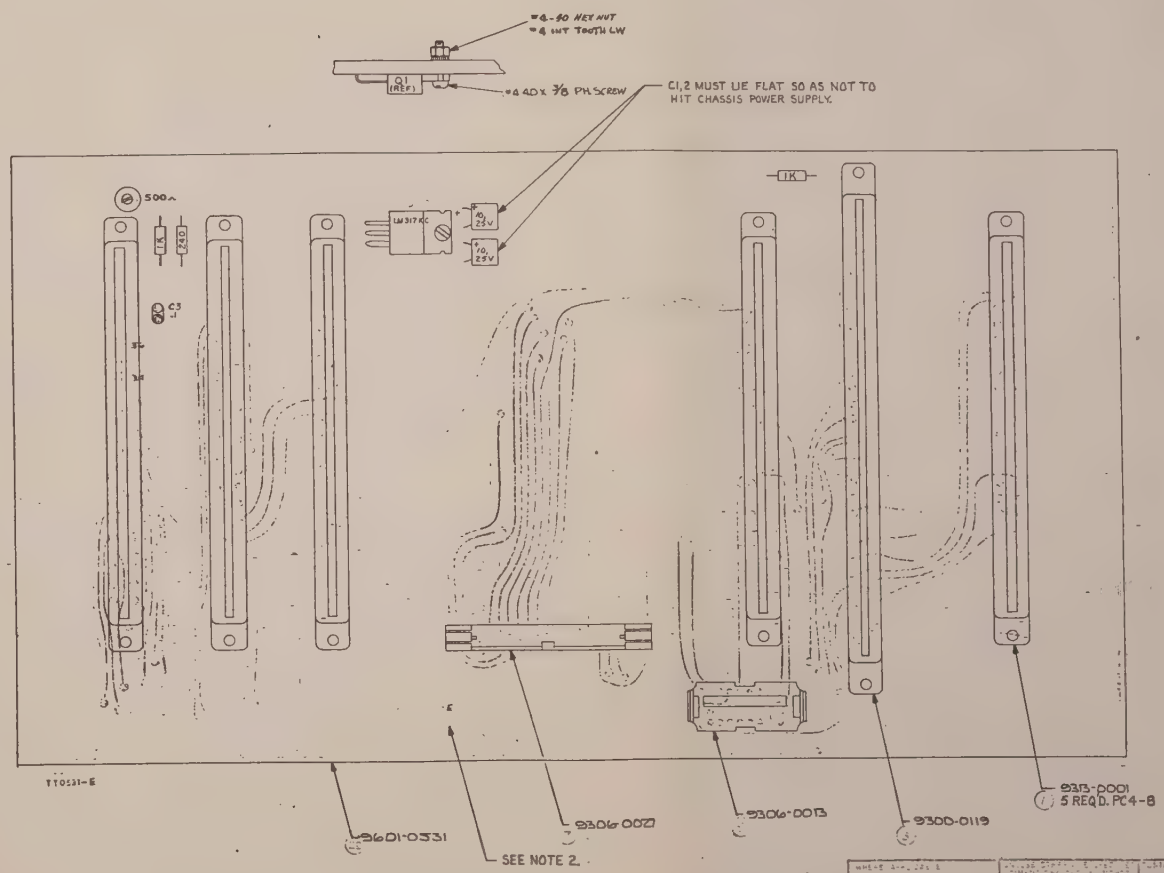
Fig. 6-8
2 of 2

tau-tron inc

DRAWING TITLE
S5102 RECEIVER
DISPLAY BOARD
SCHEMATIC

SIZE D | CODE IDENT NO | DRAWING NO. TDJ-17149 | REV C
SCALE — | S5102 | SHEET 1 OF 1

TDJ-17149



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
   B. CAPACITOR VALUES ARE IN MICROFARADS.
2. PLACE A PERMANENT REVISION LEVEL MARK ON ASSEMBLY IN THE DESIGNATED AREA.

REV	DESCRIPTION	ENG	DATE	APP
E	ADD C1,2 INSTRUCTIONS	JEH	3-17-88	SAT
F	REV PER DCN 00828, ECO-88-C3		1-19-91	
			1-27-91	
			3-27-91	

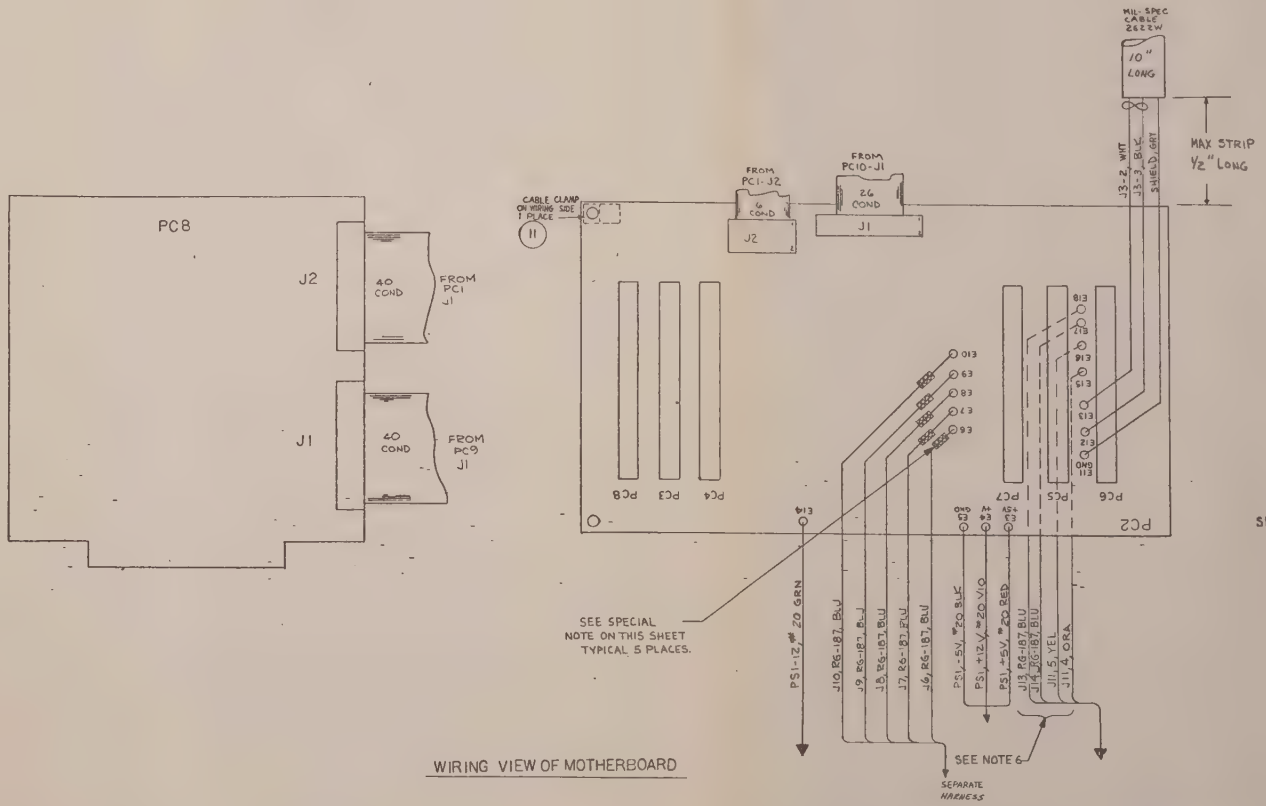
C. Smith 1-19-91
B. Cooper 1-27-91
W. Stotts 3-27-91

ASSEMBLY, RX MOTHER BOARD PCB

TEK-17156

Fig. 6-9
1 of 2

TDK-17117 F



WIRING VIEW OF MOTHERBOARD

SPECIAL NOTES:

-⊠- = SOLDER COAXIAL CABLE TO GND ETCH ON PC BOARD APPROXIMATELY AS SHOWN.

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ANGLES ±
FRACTIONS ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMALS ±
MATERIAL

CONTR NO
DR C. Smith 1-20-81
CHK E. Cooper 1-21-81
APPD [illegible] 1-22-81
APPROVED
BY DIRECTION OF

tau-tron inc Chatsworth, ca. 91311

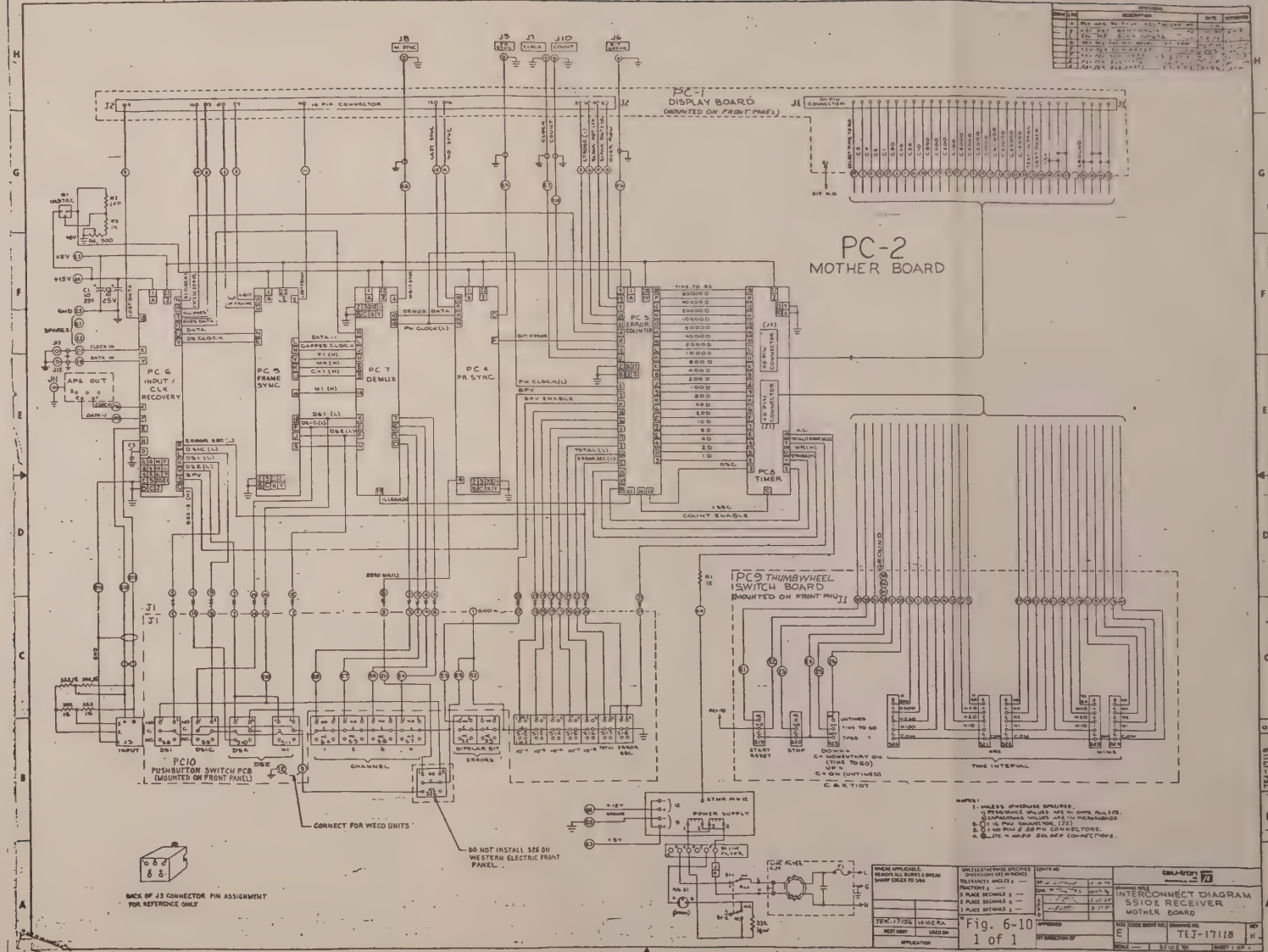
DRAWING TITLE
S5102 RX
MOTHERBOARD WIRING DIAGRAM

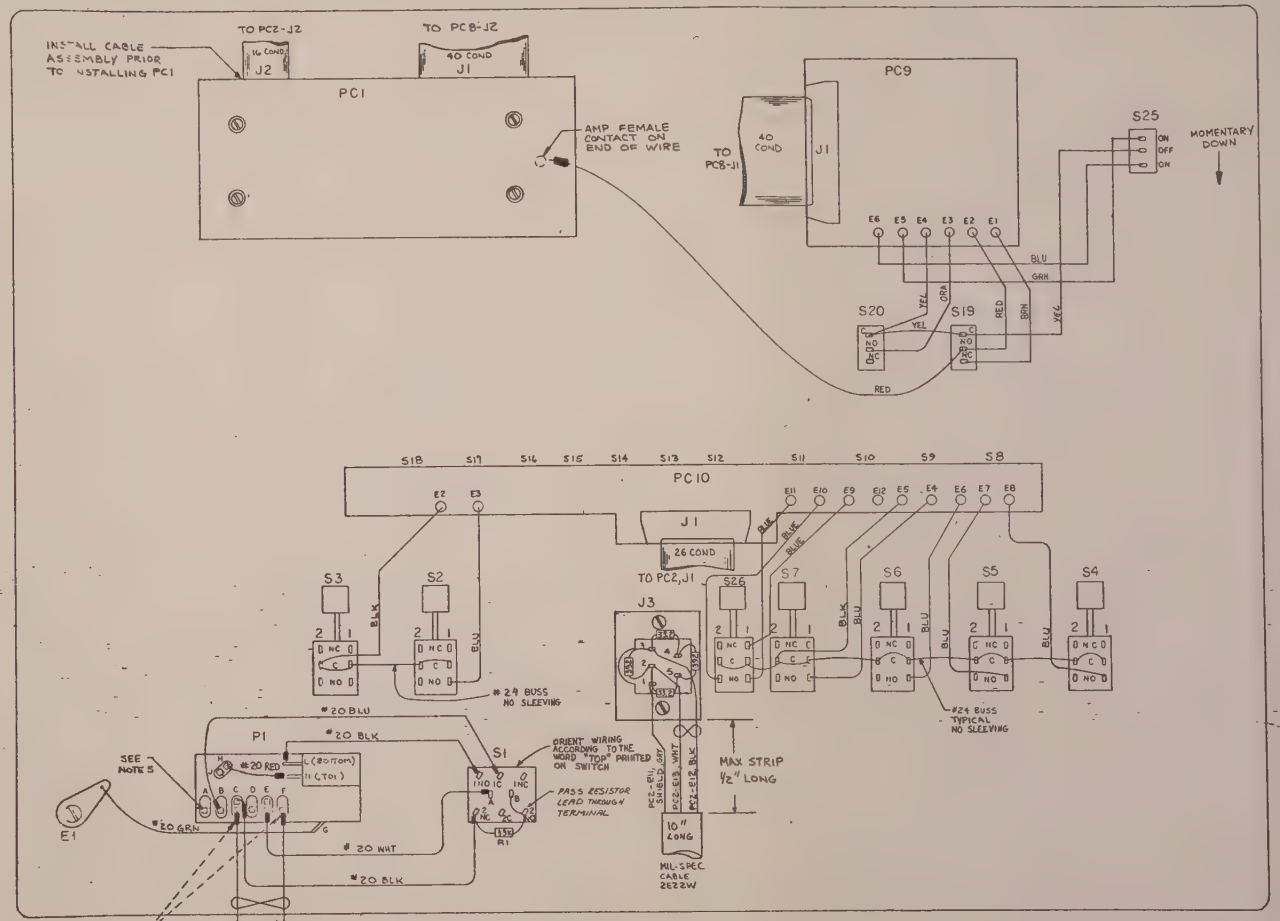
NEXT ASSY	USED ON
	S5102 RX
APPLICATION	

Fig. 6-9
2 of 2

SIZE	CODE IDENT NO	DRAWING NO.	REV
D		TDM-17240	
SCALE	S5102 - RX	SHEET 3 OF 4	

TDM-17240


PC-1
DISPLAY BOARD
(MOUNTED ON FRONT PANEL)
PC-2
MOTHER BOARD
PC 5
FRAME SYNC
PC 7
DEMUX
PC 4
PR SYNC
PC 3
ERROR COUNTER
PC 6
INPUT / CLK RECOVERY
PC 8
TIMER
PC9 THUMBWHEEL SWITCH BOARD
(MOUNTED ON FRONT PNL)
PC10
PUSHBUTTON SWITCH PCB
(MOUNTED ON FRONT PANEL)
CONNECT FOR WECO UNITS
DO NOT INSTALL SZ6 011 WESTERN ELECTRIC FRONT PANEL
BACK OF J3 CONNECTOR PIN ASSIGNMENT FOR REFERENCE ONLY
POWER SUPPLY
LINE FILTER
INTERCONNECT DIAGRAM
S5102 RECEIVER
MOTHER BOARD
TEJ-17118
TEK-17136 S5102 RA
Fig. 6-10
1 of 1



FRONT PANEL WIRING VIEW

NOTES:
1. —— DENOTES SHRINK TUBING REQUIRED.
2. WIRES TO BE #26 AWG UNLESS SPECIFIED.
3. OO DENOTES TWISTED PAIR #26 AWG.
4. RESISTORS ARE 1/8 WATT UNLESS SPECIFIED.
5. ALL UNUSED PINS ON P1 MUST BE CUT OFF AFTER WIRING. (PINS A, D, E & J)
6. RUN WIRES TO E15, 16, 17, 18 ON PC2 UNDER BOARD.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	L	REV PER ECO 00876 C.J.	4-21-81	D&E

WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64

NEXT ASSY: S5102 RX — USED ON: APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ANGLES ±
FRACTIONS ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMALS ±
MATERIAL

Fig. 6-11 1 of 1

CONTR NO.
DR L. Smith 1-20-81
CHK B. Carey 1-22-81
APPD W. Lotte 1-27-81
APPROVED
BY DIRECTION OF

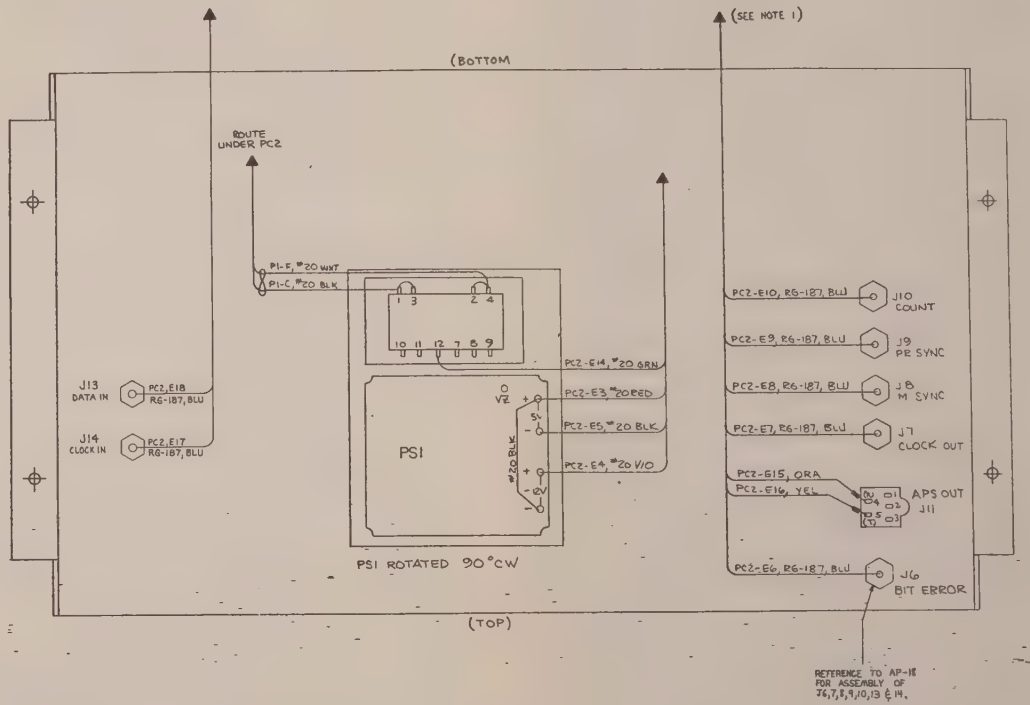
tau-tron inc. Chelmsford, Mass 01824

DRAWING TITLE
S5102 RX (COMMERCIAL UNIT)
FRONT PANEL WIRING DIAGRAM

SIZE D | CODE IDENT NO | DRAWING NO. TDM-17240 | REV 1
SCALE S5102 RX | SHEET 2 OF 4

TDM-17240

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



NOTES:
1. RUN COAXIAL WIRES BETWEEN BNC CONNECTORS & POWER SUPPLY SO WIRES DO NOT INTERFERE WITH PCB'S.

CHASSIS WIRING VIEW

TDM-17240

WHERE APPLICABLE: REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64.	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± FRACTIONS ± 3 PLACE DECIMALS ± 2 PLACE DECIMALS ± 1 PLACE DECIMALS ± MATERIAL:	CONTR NO. DR C. Smith 1-20-81 CHK R Cary 1-22-81 APPD W Little 1-23-81 APPROVED BY DIRECTION OF	tau-tron inc Chelmsford, MA 01824 DRAWING TITLE S5102 RX CHASSIS WIRING DIAGRAM
S5102 RX NEXT ASSY / USED ON APPLICATION	Fig. 6-12 1 of 1		SIZE D · CODE IDENT NO. · DRAWING NO. TDM-17240 · REV 1 SCALE · S-5102-RX · SHEET 4 OF 4

POWER-ONE Inc.
531 DAWSON DR.
CAMARILLO, CALIF. 93010
(805) 484-2806

APPLICATION DATA
Including:
1. Schematic
2. Parts Lists
3. Specification
4. Outline & Mounting Dwg.
5. General User Information

MODEL
HBB512
HBB5-3/ OVP

SPECIFICATIONS

AC Input: 115/230 VAC ± 10% 47-440 HZ (Derate Current 10% for 50 HZ operation)

Input Fusing: See Table

Line Regulation: ± .05% for a 10% input change

Load Regulation: ± .05% for a 50% load change

Output Ripple: 3mv Pk-Pk +.02% V out

Transient Response: 30u sec for 50% load change

Overload & Short Circuit Protection: Automatic current limit/foldback

Temperature Coefficient: ± .03%/°C maximum

Cooling: Units are full rated to 50°C in free air, must be derated or fan cooled when mounted in confined area

Temperature Rating: 0 - 50°C, full rated, derate linearly to 40% at 70°C

Efficiency: 55% at nominal input, full load on output

Weight: 4 lbs.

Vibration: Per Mil-Std-810B, method 514, proc. I, curve AB(to 50 HZ)

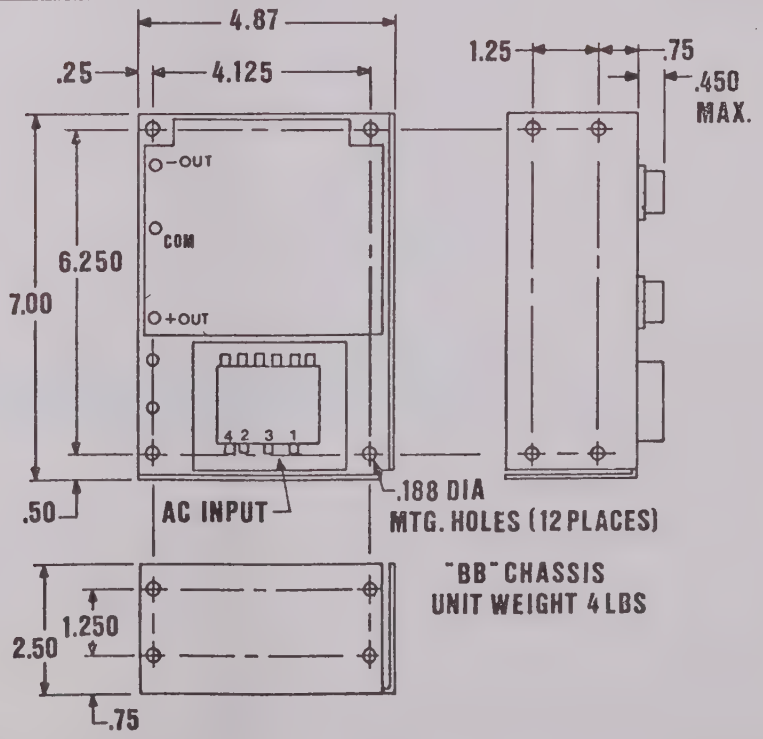
Shock: Per Mil-Std-810B, method 516, procedure V

AC Connection & Fuse Table			
For Use At	Primary Fuse At	Connect	Apply Power To
115	1A	1-3, 2-4	1 & 4
230	.5A	2-3	1 & 4

MODEL	OUTPUT RATING
HBB5-3/OVP	+5VDC @ 3A OVP preset at 6.2 ±.4VDC
HBB512	+5VDC @ 3A OVP preset at 6.2 ±.4VDC ADJ 9 to 15V @ 1.25A

2 YEAR GUARANTEE

POWER-ONE will repair or replace any power supply of its manufacture that does not perform to published specifications as a result of defective materials or workmanship for a period of 2 years from date of original purchase. No other obligations or liabilities are implied or expressed. Returns must be freight prepaid.



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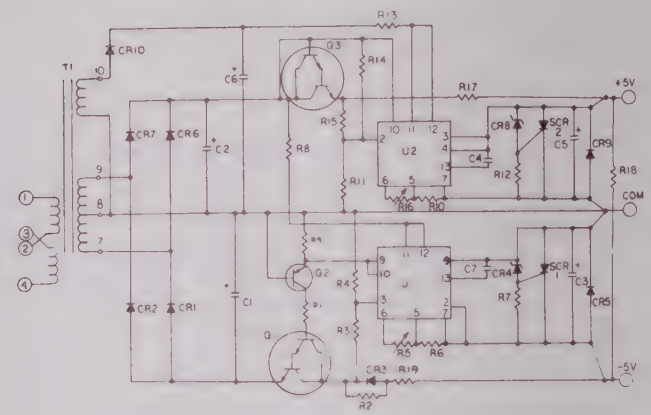
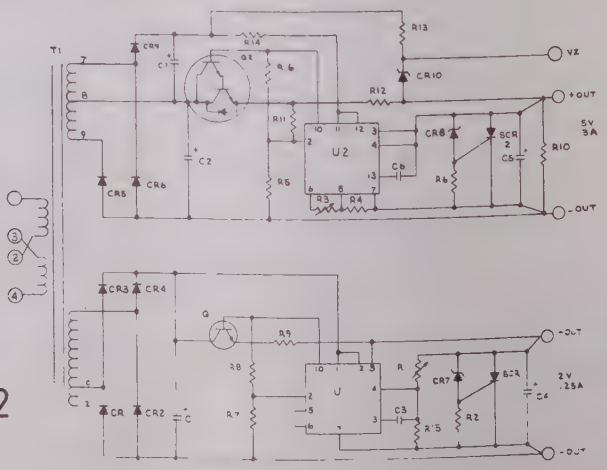
REF DES	HBB5-3/CVP	POWER-ONE P/N	DESCRIPTION
C1, 2	9000/15	102-10097	CAPACITOR ALUM ELECTROLYTIC
C6	100/35	101-10110	
C8,5	220/16	101-10107	ALUM ELECTROLYTIC
C4	.01/100	104-10095	MYLAR
C7	.1/100	104-10094	CAPACITOR MYLAR
CR5,9,10	AE1C	111-10251	DIODE, 1A, 200V
CR1,2,6,7,8	AE3B	111-10252	DIODE 3A, 100V
CR4,8	IN752A	112-10006	DIODE, ZENER, 400 mw
SCR1,2	50303L63	160-10259	SCR 3A
Q1,3	2N6055	171-10263	TRANSISTOR, POWER DARLINGTON, NPN
Q2	2N2905	172-10248	TRANSISTOR
R1,9	4.7K	151-10381	RESISTOR 1/2W CARBON
R3,8,13,14,18	270Ω	151-10351	
R11	1K	151-10365	
R4,6,10	2.2K	151-10373	
R15	240Ω	5 - 10350	
R7,12	47Ω	151-10333	1/2W CARBON
R19 17	12Ω	158-10077	RESISTOR 2W, WW, BWH
R5, R16	1.5K	155-10085	POTENTIOMETER 2W WW
U1 U2	µA723	130-10287	IC VOLTAGE REGULATOR
R2	.5Ω	151-10299	RESISTOR 1/2 W CARBON
T1	12115	082-1...5	TRANSFORMER
PCB	2089	081-12089	PRINTED CIRCUIT BOARD
CHASSIS	11101	083-11101	ALUMINUM, ALODINE COATED



REF DES	HBB5-12	POWER ONE PART NUMBER	DESCRIPTION
C1	2200/35	102-10100	CAPACITOR, ALUM ELECT
C2	9000/15	102-10097	
C4	100/35	101-10110	
C5 7	220/16	101-10107	ALUM ELECT
C3	.01/100	104-10095	MYLAR
C6	.0033/100	104-10092	CAPACITOR MYLAR
CR1 2,3 4,5 6	AE3B	111-10252	DIODE 3A, 100V
CR9	AE1C	111-10251	1A, 200V
CR8	IN752A	112-10006	DIODE ZENER 400MW
SCR 2	50303L63	160-10258	3A SCR
Q1	12500-3	171-10261	TRANSISTOR NPN
Q2	2N6055	171-10263	TRANSISTOR POWER DARLINGTON NPN
CR7 R2 ECR1			
R15	1.2K	152-10507	RESISTOR 1/8 W, MF
R4	2.8K	152-10033	1/8 W MF
R5	1K	151-10365	1/2W CARBON
R6	47Ω	10333	
R7	4.7K	10381	
R8 11, 10	240Ω	10350	
R14, 16	270Ω	151-10351	1/2 W, CARBON
R9	.22	158-10079	2W, WW BWH
R12	.12	158-10077	RESISTOR 2W, WW, BWH
R1 3	1.5K	155-10085	POTENTIOMETER 2W WW
U1 U2	µA 723	130-10287	IC VOLTAGE REGULATOR
T1	12160	082-12160	XMFR
P C BOARD	12C52	081-12052	PRINTED CIRCUIT BOARD
CHASSIS	11101	083-11101	CHASSIS ALUM



A-2

Your Feedback is Important

In fact it's necessary to help us produce an instruction manual that meets **your** needs. If you have any suggestions, corrections, or questions, we'd like to hear from you.

If you have any feedback, please complete, detach, and mail the lower card

If you would like a representative to call, require additional information, or would like to be placed on our mail list to receive **The Pulse** or other useful technical information, please complete, detach, and mail the card below.

Please —

☐ Have representative call.

☐ Add me to your mail list.

Send additional information on:

☐ Bit Error Rate Test Equipment
☐ Data/Word Generators
☐ Data Loggers
☐ High-Speed Components

My general application is _____

Name _____ Title _____

Company _____ Dept./MS _____

Address _____ City _____

State&Zip _____ Phone _____

Form 0159B-0181A

Instruction Manual Form Number _____ – _____

Comments _____

from:

Name _____ Title _____

Company _____ Dept./MS _____

Address _____ City _____

State&Zip _____ Phone _____

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CHELMSFORD, MA 01824

Repair Returns

To return a unit for repair:

1. Call the Customer Service Dept., **(617) 256-9013**, for a **Repair Authorization Number.** This will reduce administrative delays and ensure prompt return of your unit.
2. Complete and **attach one of the Repair Tags** below to your unit.
3. **Pack the unit** in the original shipping carton and packaging materials, if available. Otherwise use a double-walled carton (test strength of 350 lb) and shock absorbing material such as bubble wrap to prevent the unit from moving in the carton during transit. Seal with heavy paper tape.
4. **Send to:**

   Tau-Tron
   27 Industrial Ave.
   Chelmsford, MA 01824
   atten: Customer Service

Repair Tag

Repair Authorization Number _____

Model _____ **Serial Number** _____

☐ Warranty repair ☐ Dead on arrival ☐ Repair ☐ Modification ☐ Recalibration

Symptoms: _____

_____

Name _____ Title _____

Company _____ Dept./MS _____

Address _____ City _____

State&Zip _____ Phone _____

Form 0163-1181A

Repair Tag

Repair Authorization Number _____

Model _____ **Serial Number** _____

☐ Warranty repair ☐ Dead on arrival ☐ Repair ☐ Modification ☐ Recalibration

Symptoms: _____

_____

Name _____ Title _____

Company _____ Dept./MS _____

Address _____ City _____

State&Zip _____ Phone _____

Form 0163-1181A

Tau-Tron, Inc. 27 Industrial Ave., Chelmsford, MA 01824